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(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

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(72)Inventor : SHIMOYAMA KOJI  
NAKAO KEIICHI  
KIMURA RYO  
YONEDA NAOTSUGU

(30)Priority

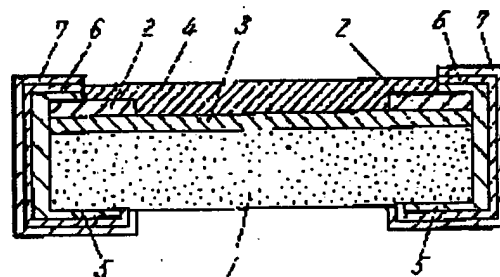
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## (54) CHIP RESISTOR AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To realize low resistance and low TCR (temperature coefficient) characteristics, and in addition, high precision and high reliability, in a chip resistance used for a circuit part of various electrical equipment.

SOLUTION: This chip resistor comprises a substrate 1, a resistance layer 3 of copper/nickel alloy formed at least on one side of the substrate 1, upper surface electrode layers 2 which are formed on both end parts of the resistance layer 3, respectively, so as to be brought into surface-contact with the top surface, and an end surface electrode layer 5 provided so as to cover the top surface electrode layer 2. In particular, since joint of the resistance layer 3 and the top surface electrode layer 5 is metal joint, no such impurity affecting on characteristics exists on an interface between them, thereby the chip resistor of excellent heat-resisting property, low resistance and low TCR characteristics is realized.



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CLAIMS

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[Claim(s)]

[Claim 1] An insulating substrate and the resistive layer which consists of the copper / nickel alloy powder, and the glass frit which were prepared at least in one side of this insulating substrate, The top-face electrode layer of the pair prepared in the both ends of this resistive layer so that field contact might be carried out from a top face, respectively, The chip resistor which is equipped with the end-face electrode of the pair prepared in the both-sides side of said insulating substrate so that a part of field electrode layer [ at least ] may besides be covered, and is characterized by junction in said resistive layer and said top-face electrode layer being metal junction.

[Claim 2] The chip resistor according to claim 1 characterized by the resistance of a top-face electrode layer being lower than a resistive layer.

[Claim 3] The chip resistor according to claim 2 characterized by a top-face electrode layer consisting of a copper electrode or a silver electrode.

[Claim 4] An insulating substrate and the inferior-surface-of-tongue electrode layer of the pair prepared in the both ends of at least one side of this insulating substrate, The resistive layer which consists of the copper / nickel alloy powder, and the glass frit which were prepared so that the inferior-surface-of-tongue electrode layer of this pair might be connected, The top-face electrode layer of the pair prepared in said inferior-surface-of-tongue electrode layer of this resistive layer, and the both ends which counter so that field contact might be carried out from a top face, respectively, The chip resistor which is equipped with the end-face electrode of the pair prepared in the both-sides side of said insulating substrate so that a part of field electrode layer [ at least ] may besides be covered, and is characterized by junction in said resistive layer and said top-face electrode layer being metal junction.

[Claim 5] The chip resistor according to claim 4 characterized by the resistance of a top-face electrode layer and an inferior-surface-of-tongue electrode layer being lower than a resistive layer.

[Claim 6] The chip resistor according to claim 4 characterized by a top-face electrode layer and an inferior-surface-of-tongue electrode layer consisting of a copper electrode or a silver electrode.

[Claim 7] The process which forms the resistive layer which becomes at least one side of an insulating substrate from copper / nickel alloy powder, and a glass frit, The process which forms and calcinates the top-face electrode layer of a pair to the both ends of this resistive layer so that field contact may be carried out from a top face, respectively, The manufacture approach of the chip resistor characterized by having the process which forms the end-face electrode of a pair in the both-sides side of said insulating substrate so that a part of top-face electrode layer [ at least ] by which sintering formation was carried out may be covered, and the resistive layer by which sintering formation was carried out, and the top-face electrode layer being joined by metal junction.

[Claim 8] The manufacture approach of the chip resistor according to claim 7 characterized by carrying out sintering formation at the temperature of 600-1000 degrees C under the reducing atmosphere which is under nitrogen-gas-atmosphere mind about a resistive layer and a top-face electrode layer, or contained hydrogen.

[Claim 9] The process which forms the inferior-surface-of-tongue electrode layer of a pair in the both

ends of at least one side of an insulating substrate, The process which forms the resistive layer which consists of copper / nickel alloy powder, and a glass frit so that the inferior-surface-of-tongue electrode layer of this pair may be connected, The process which forms and calcinates the top-face electrode layer of a pair to the both ends of this resistive layer so that field contact may be carried out from a top face, respectively, It has the process which forms the end-face electrode of a pair in the both-sides side of said insulating substrate so that a part of top-face electrode layer [ at least ] by which sintering formation was carried out may be covered. The manufacture approach of the chip resistor characterized by the inferior-surface-of-tongue electrode layer, resistive layer and resistive layer by which sintering formation was carried out, and the top-face electrode layer being joined by metal junction, respectively.

[Claim 10] The manufacture approach of the chip resistor according to claim 9 characterized by carrying out sintering formation at the temperature of 600-1000 degrees C under the reducing atmosphere which is under nitrogen-gas-atmosphere mind about a resistive layer and a top-face electrode layer, or contained hydrogen.

[Claim 11] The baking resistor layer which is prepared in both sides of a ceramic substrate and consists of copper / nickel alloy powder at least and by which sintering formation was carried out, The terminal electrode prepared so that a part of each both ends of the baking resistor layer of these both sides might be covered at least, The sintering particle diameter of the baking resistor layer which was equipped with the end-face electrode prepared in the both-sides side of said ceramic substrate so that a part of each both ends of this terminal electrode might be covered at least, and was prepared at least in one side of said ceramic substrate by 30 micrometers or less And the chip resistor characterized by the thickness being 40 micrometers or less.

[Claim 12] The chip resistor characterized by having the metallic foil which consists of copper / nickel or nickel / chromium at least, and the baking resistor layer which is prepared on this metallic foil and consists of copper/nickel at least, and by which sintering formation was carried out, and for the sintering particle diameter of said baking resistor layer being 30 micrometers or less, and that thickness being 40 micrometers or less.

[Claim 13] The metallic foil which was prepared at least in one side of a ceramic substrate and which consists of copper / nickel or nickel / chromium at least, The baking resistor layer which is prepared on this metallic foil and consists of copper nickel at least and by which sintering formation was carried out, The terminal electrode of the pair prepared so that a part of each both ends of this baking resistor layer might be covered at least, The chip resistor characterized by having the end-face electrode prepared in the both-sides side of said ceramic substrate so that a part of each both ends of this terminal electrode may be covered at least, and for the sintering particle diameter of said baking resistor layer being 30 micrometers or less, and that thickness being 40 micrometers or less.

[Claim 14] The chip resistor according to claim 13 characterized by using the metal wire which replaces with a metallic foil and consists of copper / nickel or nickel / chromium at least.

[Claim 15] The metallic foil which was prepared in one side of a ceramic substrate and which consists of copper / nickel or nickel / chromium at least, The baking resistor layer which is prepared in another one side and consists of copper/nickel at least and by which sintering formation was carried out, The terminal electrode of the pair prepared so that a part of each both ends of this baking resistor layer might be covered at least, It has the end-face electrode prepared in the both-sides side of said ceramic substrate so that a part of a part of each both ends of this terminal electrode and both ends of a metallic foil might be covered at least. The sintering particle diameter of said baking resistor layer by 30 micrometers or less And the chip resistor characterized by the thickness being 40 micrometers or less.

[Claim 16] The metal wire which was prepared in one side of a ceramic substrate and which consists of copper / nickel or nickel / chromium at least, The baking resistor layer which is prepared in another one side and the top face of said metal wire, and consists of copper/nickel at least and by which sintering formation was carried out, The terminal electrode prepared so that a part of each both ends of the baking resistor layer of these both sides might be covered at least, It has the end-face electrode prepared in the both-sides side of said ceramic substrate so that a part of each both ends of this terminal electrode might be covered at least. One [ at least ] sintering particle diameter of said two baking resistor layers by 30

micrometers or less And the chip resistor characterized by the thickness being 40 micrometers or less.  
[Claim 17] The chip resistor indicated by either of claims 11-16 characterized by leaving a part of the end-face electrode [ at least ], and covering the whole by resin.

[Claim 18] The process which forms in both sides of a ceramic substrate the resistor layer which consists of copper / nickel alloy powder at least, The process which forms a terminal electrode so that a part of each both ends of this resistor layer may be covered at least, The process which calcinates this after forming an end-face electrode in the both-sides side of said ceramic substrate so that a part of each both ends of this terminal electrode may be covered at least, The manufacture approach of the chip resistor characterized by forming in thickness within the limits which can perform trimming according the thickness of the resistor layer which was equipped with the process which trims this calcinated resistor, and was prepared at least in one side of said ceramic substrate to laser.

[Claim 19] The manufacture approach of the chip resistor characterized by forming in thickness within the limits which can perform trimming according the thickness of a resistor layer to laser when forming the resistor layer which consists of copper/nickel at least on the metallic foil which consists of copper / nickel or nickel / chromium at least and performing trimming after baking.

[Claim 20] The process which forms the metallic foil or metal wire which becomes at least one side of a ceramic substrate from copper / nickel or nickel / chromium at least, The process which forms the resistor layer which consists of copper/nickel at least on this metallic foil or a metal wire, The process which forms the terminal electrode of a pair so that a part of both ends of this resistor layer may be covered at least, The process which calcinates this after forming an end-face electrode in the both-sides side of said ceramic substrate so that a part of both ends of a part of each both ends of this terminal electrode and a metallic foil, or a metal wire may be covered at least, The manufacture approach of the chip resistor characterized by forming in thickness within the limits which can perform trimming according the thickness of the resistor layer which was equipped with the process which trims this calcinated resistor, and was prepared at least in one side of said ceramic substrate to laser.

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DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] The type section Fig. of the chip resistor in the gestalt of operation of the 1st of this invention

[Drawing 2] The production process Fig. of the gestalt of this operation

[Drawing 3] The type section Fig. of the chip resistor in the gestalt of operation of the 3rd of this invention

[Drawing 4] The type section Fig. of the chip resistor in the gestalt of operation of the 4th of this invention

[Drawing 5] The type section Fig. of the chip resistor in the gestalt of operation of the 5th of this invention

[Drawing 6] The type section Fig. of the chip resistor in the gestalt of operation of the 6th of this invention

[Drawing 7] The type section Fig. of the chip resistor in the gestalt of operation of the 7th of this invention

[Drawing 8] The type section Fig. of the chip resistor in the gestalt of operation of the 8th of this invention

[Drawing 9] The type section Fig. of the chip resistor in the gestalt of operation of the 9th of this invention

[Drawing 10] The perspective view showing signs that resin coating was performed as a protective layer in the chip resistor in the gestalt of operation of the 4th of this invention

[Drawing 11] The same section notching sectional view

[Drawing 12] The perspective view showing the configuration of the conventional chip resistor

[Drawing 13] This A-A' sectional view

[Description of Notations]

1 Substrate

2 Top-Face Electrode Layer

3 Resistive Layer

4 Protective Coat Layer

5 End-Face Electrode Layer

6 Nickel Plating Film

7 Solder Plating Film

8 Inferior-Surface-of-Tongue Electrode Layer

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the chip resistor which has low resistance and a low TCR property especially, and its manufacture approach about the chip resistor widely used for an electronic circuitry.

[0002]

[Description of the Prior Art] The miniaturization of these electronic equipment and high performance-ization are referred to as dependent on the miniaturization of the chip mold electronic parts with the steadily increasing need of small electronic equipment used for this, and high performance-ization, and it will not be an overstatement from now on so that it may be represented by a cellular phone, a movie, the notebook computer, etc. in recent years. The constituent which uses as a principal component the ruthenium acid bismuth which are ruthenium oxide and its multiple oxide as a thick film resistor, and lead ruthenate is known (for example, refer to JP,58-37963,B), and it is used in various fields.

[0003] An example of the manufacture approach of the conventional chip resistor is explained based on a drawing. Drawing 12 is the perspective view showing an example of the structure of the conventional square shape chip resistor, and drawing 13 is a sectional view in the A-A' section of drawing 12. First, next, the manufacture approach of this kind of square shape chip resistor forms the up electrode 11 in the top face of the alumina substrate 10 of the shape of a chip which consists of an alumina 96%, and it forms a resistor 12 in a part of top face of the alumina substrate 10 so that it may connect with the above-mentioned up electrode, and generally, it forms in it the protective coat 14 which consists of lead borosilicate system glass so that this resistor 12 may be covered further completely. Generally, the above-mentioned protective coat 14 is formed by calcinating at the elevated temperature of 500-800 degrees C, after screen-stencil performs pattern formation.

[0004] Next, the end-face electrode 13 which becomes with the thick film of Ag system is formed in the edge surface part of the above-mentioned alumina substrate 10 so that the up electrode 11 may be connected, and this end-face electrode 13 is formed by generally calcinating at the elevated temperature near 600 degree C at this time. In order to secure the dependability when soldering at the end, nickel plating film 15 was formed by electroplating so that the above-mentioned end-face electrode 13 might be covered, and the solder plating film 16 was formed so that this nickel plating film 15 might be covered, and the square shape chip resistor has been obtained.

[0005] Although the thick-film glaze resistor ingredient which generally uses ruthenium oxide as a principal component as an electric conduction particle used as a resistor in the chip resistor manufactured by the above manufacture approaches is used With the resistor ingredient which consists only of this ruthenium oxide, since the temperature coefficient of resistance (henceforth TCR) which shows the temperature change of resistance became large, it needed to use by adding TCR adjustment material, such as a metallic oxide, by making it the low value of less than about \*\*50 ppm/degree C.

[0006] However, when such a resistor ingredient was used, since the specific resistance of ruthenium oxide was high, it was difficult [ it ] to form the chip resistor which has the low resistance of 1ohm or

less. Therefore, it is JIS as a low resistor ingredient 1ohm or less. The chip resistor using copper/nickel alloy with a small temperature coefficient of resistance which is indicated by C2521 and this C2532 is proposed.

[0007] That is, after printing the structure of processing the configuration of a foil or a plate and sticking this alloy ingredient on an alumina substrate, and the resistive paste which kneaded copper powder, nickel powder, and a glass frit with the organic vehicle on an alumina substrate, the thing of the structure which form the alloy film be propose by calcinating in an inert atmosphere ( refer to JP,2-308501,A and JP,3-270104,A).

[0008]

[Problem(s) to be Solved by the Invention] However, in the case of the former, the approach of processing an alloy foil or an alloy plate had a limitation, while the configuration of a chip was progressing towards the miniaturization increasingly, and trimming could not use laser, but there was a limitation in polishing, and since it was [ still in cost / the printing approach ] disadvantageous, it was seldom the thing excellent in mass-production nature.

[0009] moreover , since in the case of the latter glass be use for adhesion of the resistor film and a substrate or adjustment of resistance and many components other than copper and nickel be contained , while the temperature coefficient differed from the physical properties value of copper nickel alloys , since the diffusion behavior to the inside of a metal component or a sintering particle interface changed with baking conditions , the glass component had the technical problem that the stable resistance property be hard to be acquire .

[0010] Furthermore, in order that the property of the terminal electrode of the electric supply section and the structure of a resistor / electrode interface might influence the property as a resistor greatly in the mull technique using copper and nickel powder, as resistance, even 100mohm was a limitation, and it was difficult to realize still lower resistance.

[0011] While the configuration of recent years and a chip resistor serves as an inclination of a miniaturization increasingly like the above-mentioned, the requests of a chip resistor which are the low resistance used for current detection of an electronic circuitry etc., and have a low TCR property are mounting increasingly, and, in addition to low resistance and a low TCR property, it is anxious for a chip resistor with which are satisfied of high degree of accuracy and high-reliability from the engine performance of an application in which it is used further.

[0012] This invention aims at offering the chip resistor which solves the technical problem mentioned above, and has especially 1ohms or less of the low resistance not more than 100mohm and low TCR properties in response to the above-mentioned request, and has high-reliability, and its manufacture approach.

[0013]

[Means for Solving the Problem] The resistive layer which this invention becomes from the copper/nickel alloy formed at least in one side of an insulating substrate and this insulating substrate, The top-face electrode layer of the pair formed so that field contact of each of the both ends of this resistive layer might be carried out from a top face, Since it is the chip resistor which has the end-face electrode of the pair formed in the both ends of said insulating substrate as a part of field electrode layer [ at least ] is besides covered, and junction of a resistive layer and a top-face electrode layer is especially performed by metal junction, It is not placed between interfaces by impurity which affects a property, but the chip resistor which are low resistance and a low TCR property, and was excellent in thermal resistance is obtained.

[0014]

[Embodiment of the Invention]

(Gestalt 1 of operation) Drawing 1 shows the cross section of the chip resistor in the gestalt of operation of the 1st of this invention. In drawing, 3 is a resistive layer and is carrying out printing formation with thick-film techniques, such as screen-stencil, using the resistive paste which becomes one side of the rectangular insulating substrate (it is only hereafter called a substrate) 1 from an alloy presentation as shown in (Table 1). Next, printing formation of the top-face electrode layer 2 is carried out by the same

approach as a resistive layer 3 so that field contact may be carried out with a resistive layer 3 to the both ends of the pair which counters a substrate 1, and coincidence baking of this resistive layer 3 and the top-face electrode layer 2 is carried out in neutral atmosphere or reducing atmosphere. Then, the end-face electrode layer 5 is formed in the part which is not covered with the both ends of a pair to which the protective coat layer 4 is formed so that a part of this resistive layer 3 may be covered, and a substrate 1 counters in the shape of a KO character, and the protective coat layer 4 of a resistive layer 3.

Furthermore, the wrap nickel plating film 6 is formed for this end-face electrode layer 5, and the solder plating film 7 is formed on this nickel plating film 6.

[0015] Below, the production approach of a chip resistor is explained in full detail. Resistive paste used as the inorganic composition the mixed fine particles which added the glass frit to this using copper / nickel alloy powder (atomizing powder with a mean particle diameter of 5 micrometers). The glass frit made this the organic vehicle constituent using what was comparatively alike, and added and melted 5% of the weight of the ethyl cellulose which is an organic binder for lead borosilicate glass by terpeneol for the vehicle component to the metal powder. These inorganic compositions and an organic vehicle constituent were kneaded with 3 rolls, and it considered as resistive paste.

[0016] Next, top-face electrode paste made this the organic vehicle constituent at the vehicle component using what melted the ethyl cellulose which is an organic binder by terpeneol using copper powder (mean particle diameter: 2 micrometers) or silver dust (mean particle diameter: 5 micrometers). These inorganic compositions and an organic vehicle constituent were kneaded with 3 rolls, and it considered as top-face electrode paste.

[0017] Thus, while printing a resistor pattern on a substrate 1 (96% alumina substrate) using the screen version and drying said adjusted resistive paste for 10 minutes at the temperature of 100 degrees C, it printed continuously to the predetermined pattern as uses the screen version for the top face of a resistor pattern and shows said top-face electrode paste to drawing 1, and was made to dry for 10 minutes at the temperature of 100 degrees C. Next, coincidence baking of a resistor and an electrode is performed in the profile to which this substrate 1 is made as for nitrogen-gas-atmosphere mind baking, coincidence formation of a resistive layer 3 and the top-face electrode layer 2 is carried out, after dividing a substrate 1 further and preparing a copper electrode as an end-face electrode 5, as a protective coat of a resistive layer 3, the protective coat layer 4 was formed by screen-stencil, and resin hardening of the epoxy resin was carried out on 160 degrees C and the conditions for 30 minutes. It evaluated about the temperature coefficient (TCR) and dependability (the elevated-temperature shelf test, spalling test) of the resistance of the made resistor element, and resistance.

[0018] Moreover, after forming the copper electrode or silver electrode which contains a glass frit as an up electrode 11 so that it may become structure as shown in drawing 13 as an example of a comparison, After printing what pasted an alloy powder, glass, and an organic vehicle like the above on the alumina substrate 10 (96% alumina substrate) and making it dry for 10 minutes at the temperature of 100 degrees C, it heated on the baking conditions shown in (Table 1) under N2 ambient atmosphere, and the resistor was calcinated.

[0019] Next, the evaluation approach of the resistor after baking is shown. After resistance put the sample on the ambient atmosphere of RH gently more than for 30 minutes temperature [ of 25\*\*2 degrees C ], and humidity 65\*\*10%, it was calculated by 4 terminal method. Moreover, after the TCR property put the resistor into the thermostat and put the sample on the temperature ambient atmosphere gently more than for 30 minutes, it measured the resistance of 25 degrees C and 125 degrees C, and asked for the rate of change.

[0020] The spalling test which is dependability evaluation criteria had two chambers (-45 degrees C, +150 degrees C) beforehand set as predetermined temperature, and immediately after holding for 30 minutes to one chamber, the rate of a change in resistance after 500 cycle \*\*\*\*\* was evaluated for the trial put to the chamber of another side for 30 minutes. Moreover, the elevated-temperature shelf test evaluated the rate of a change in resistance after leaving it in the chamber held at 150 degrees C for 1000 hours.

[0021] Moreover, the crystal structure was clarified for the alloy layer cross-section section of the



produced resistor using X-ray diffractometer.

[0022]

[Table 1]

合金組成 Cu/Ni (重量比)	比較例 70/30 +ガラスフリット5wt%		70/30 +ガラスフリット5wt%					
	銅粉+ ガラスフリット 5wt%	銀粉+ ガラスフリット 5wt%						
上部電極								
上面電極			銅電極			銀電極		
焼成温度 (℃)	900	850	600	900	1000	600	800	850
焼成時間 (時間)	10	10	30	10	10	10	10	10
抵抗値 (mΩ)	60	80	70	40	10	90	70	60
T C R (ppm/℃)	15	40	-10	10	20	-20	10	40
熱衝撃試験 -40℃~ +85℃ 500サイクル	±4%	±5%	±0.4%	±0.2%	±0.1%	±0.5%	±0.3%	±0.2%
高温放置 (150℃- 1000時間)	±5%	±6%	±0.7%	±0.4%	±0.2%	±0.9%	±0.5%	±0.3%

[0023] From the result of (Table 1), the resistor film of the example of a comparison produced with the conventional structure is understood that connection with an up electrode is inadequate as quality as a resistor of which high degree of accuracy and high-reliability are required. It turned out that much existence of a glass frit, many openings, etc. will be seen in the interface of a resistor 12 and the up electrode 11 if cross-section observation of the membrane quality at that time is carried out, and the eburnation by sintering is not fully progressing.

[0024] It turned out that the crystal structure without the clear interface which an impurity did not intervene since the interface of the resistive layer 3 produced by this invention approach on the other hand and the top-face electrode layer 2 did not contain the glass frit, and was combined by coincidence sintering by the metal diffusion of the top-face electrode layer 2 and a resistive layer 3 is realizable. This is considered that the thermal stability having a diffusion layer without the interface carried out clearly excelled [ thermal stability ] in the dependability side is shown by being spread by coincidence sintering in the copper / nickel alloy layer copper or whose silver is a resistive layer. When the metal membrane after sintering was analyzed with X-ray diffractometer, it turned out that uniform copper / nickel alloy layer are formed. Furthermore, when membrane quality was observed with the scanning electron microscope, it turned out that the precise sintering film of an opening which is not almost is obtained.

[0025] Next, according to the production process Fig. of drawing 2, the concrete manufacture approach of this chip resistor is explained.

[0026] The resistor constituent into which the ratio of a glass frit was changed was mixed with copper / nickel alloy powder by 3 roll mills, and the resistive paste of the viscosity of 200,000-250,000 pascals and a second was adjusted (Step1).

[0027] This paste was screen-stenciled to the alumina substrate, it dried (resistor size: 2mm angle, desiccation thickness: 40 micrometer), the resistor was formed (Step2), copper powder (mean particle diameter: 2 micrometers) or silver dust (mean particle diameter: 5 micrometers), and an organic vehicle were kneaded by 3 roll mills as a top-face electrode layer, and the electrode paste of the viscosity of 200,000-250,000 pascals and a second was adjusted (Step3). Desiccation formation (desiccation thickness: 30 micrometers) is screen-stenciled and carried out so that it may become the structure which carries out field contact on the top face of said resistor as shown in drawing 1 R> 1 using this electrode

paste (Step4). Then, under nitrogen-gas-atmosphere mind, it held for 10 minutes, and calcinated at 900 degrees C, and the resistive layer 3 and the top-face electrode layer 2 were produced (Step5).

[0028] Subsequently, it applied so that it might become about 50-100 micrometers of thickness to an end face using commercial copper electrode paste as an end-face electrode, and it calcinated for 10 minutes at 800 degrees C by nitrogen-gas-atmosphere mind, and the end-face electrode layer 5 was formed (Step6). After that, by the YAG laser, the epoxy resin paste (Step8) was continuously carried out and (Step7) hardened [ trimming / cutting / printed and ] on the resistive layer as a protective coat in the resistive layer 3 (hardening thickness: 40 micrometers and 150 degrees C 30-minute hardening maintenance), and the protective coat layer 4 was produced (Step9).

[0029] Then, in order to consider as a chip, the design which raises (Step 10 and 11) and the solder wettability at the time of mounting was carried out by processing the nickel plating 6 and the solder plating 7 to an end face.

[0030] As for the resistor obtained by such manufacture approach, it turns out that it has sufficient dependability in heat-resistant properties, such as elevated-temperature neglect and a spalling test, so that clearly from (Table 1). Having the alloyed diffusion layer without having the interface of a metal layer clearly as a stable reason in an elevated temperature, and the chip resistor which was excellent in thermal resistance with low resistance and a low TCR property since the glass frit which is an impurity was not included in a top-face electrode layer were realizable.

[0031] Moreover, although the temperature coefficient of resistance (TCR property) could be adjusted in 400--200ppm/degree C by generally changing the alloy ratio of copper/nickel, with the gestalt 1 of this operation, it was stopped in the range of 40--20ppm/degree C also including burning-temperature conditions, and resistance has also been covered to the low resistance range to 10mohm. And the bond strength demanded as a resistor is also excellent. Moreover, also in other reliability evaluation, it had the endurance as practically sufficient resistor.

[0032] In addition, although the resin paste was used with the gestalt of this operation as a protective coat, even if it uses the glass paste usually used often, it cannot be overemphasized that the same effectiveness is acquired.

[0033] (Gestalt 2 of operation) the alloy powder shown in (Table 2) below -- a mixing ratio -- the chip resistor obtained by carrying out printing baking like the gestalt 1 of operation by the firing environments which shows the resistive paste adjusted by the same approach as the gestalt 1 of operation in (Table 2) is explained using the thing of a presentation.

[0034] Thus, it evaluated about the temperature coefficient (TCR) of the resistance of the produced chip resistor, and resistance, and dependability (elevated-temperature neglect, spalling test).

[0035] Moreover, after printing using the screen version what was pasted like the alloy powder, the glass frit, and the gestalt 1 of operation of an organic vehicle on the substrate 10 with which the up electrode 11 as shown in drawing 13 as an example of a comparison was formed and making it dry for 10 minutes at the temperature of 100 degrees C, it heated at 1000 degrees C under N2 ambient atmosphere, and the resistor was calcinated. Then, the end-face electrode and the protective coat were formed like the gestalt 1 of operation, and it considered as the resistor.

[0036] The evaluation approach of the resistor after baking was also searched for by the same approach as the gestalt 1 of operation. The result is shown in (Table 2).

[0037]

[Table 2]

合金組成 Cu/Ni (重量比)	比較例 40/60 +ガラスフリット3 wt%		40/60 +ガラスフリット3 wt%					
上部電極	銅粉+ ガラスフリット 5wt%	銀粉+ ガラスフリット 4 wt%						
上面電極			銅電極			銀電極		
焼成雰囲気	水素1%一気素雰囲気 (還元雰囲気)							
焼成温度 (℃)	900	850	600	900	1000	600	800	850
焼成時間 (時間)	10	10	30	10	10	10	10	10
抵抗値 (mΩ)	50	70	60	30	10	80	60	50
TCR (ppm/℃)	35	50	-30	20	15	-15	10	30
熱衝撃試験 -40℃～ +85℃ 500サイクル	±5%	±6%	±0.7%	±0.3%	±0.2%	±0.6%	±0.5%	±0.3%
高温放置 (150℃- 1000時間)	±6%	±7%	±0.5%	±0.3%	±0.2%	±0.8%	±0.4%	±0.3%

[0038] The interface of the resistive layer 3 produced by the gestalt approach of this operation and the top-face electrode layer 2 has realized the crystal structure without the clear interface which an impurity did not intervene and was combined by coincidence sintering by the metal diffusion of the top-face electrode layer 2 and a resistive layer 3 so that clearly from (Table 2). This shows the thermal stability having a diffusion layer without an interface by coincidence sintering excelled [ thermal stability ] in the dependability side. These things show that have low resistance and a low TCR property and the chip resistor in which the property excellent in dependability is shown is obtained.

[0039] In addition, when using a silver electrode, if it is the range whose burning temperature is 600-850 degrees C, repeatability is good [ if burning temperature is the range which is 600-1000 degrees C when using a copper electrode as a top-face electrode layer, repeatability is good about resistance or a temperature coefficient of resistance, and ] about resistance or a temperature coefficient of resistance. However, since alloying with silver and the copper of a resistive layer takes place at low temperature when using a silver electrode, it is seldom raised to an elevated temperature. Moreover, low resistance is further realizable by calcinating in reducing atmosphere from the inside of nitrogen-gas-atmosphere mind as a firing environments.

[0040] (Gestalt 3 of operation) Drawing 3 shows the cross section of the chip resistor of the gestalt of operation of the 3rd of this invention. In this chip resistor, printing baking is carried out with thick-film techniques, such as screen-stencil, and the inferior-surface-of-tongue electrode layer 8 is formed in the both ends of the pair which counters a substrate at one side of the rectangular substrate 1. the inferior-surface-of-tongue electrode layer 8 -- as a metal powder -- copper or silver dust -- using -- as a glass frit -- lead borosilicate glass -- a metal powder -- receiving -- 3wt(s)% -- the added electrode paste was used. Next, with thick-film techniques, such as screen-stencil, as shown in drawing 3 using the resistive paste which becomes the alloy presentation shown in (Table 3), printing formation of the resistive layer 3 is carried out on the inferior-surface-of-tongue electrode layer 8. Next, printing formation of the top-face electrode layer 2 is carried out by the same approach as a resistive layer 3 so that field contact may be carried out with a resistive layer 3 to the both ends of the pair which counters a substrate 1. And it forms by carrying out coincidence baking of this resistive layer 3 and the top-face electrode layer 2 in neutral atmosphere or reducing atmosphere. Then, formation of a protective coat and an end-face electrode is formed by the same approach as the gestalt 1 of operation.

[0041] The evaluation same also about the temperature coefficient (TCR) of the resistance of the made chip resistor and resistance and dependability (an elevated-temperature shelf test, spalling test) as the gestalt 1 of operation was carried out.

[0042]

[Table 3]

合金組成 Cu/Ni (質量比)	比較例 70/30 +ガラスフリット5wt%		70/30 +ガラスフリット5wt%					
	銅粉+ ガラスフリット 5wt%	銀粉+ ガラスフリット 5wt%						
上部電極								
上面電極			銅電極					
下面電極			銅粉+ガラスフリット4%					
焼成温度 (℃)	900	850	600	900	1000	600	900	1000
焼成時間 (時間)	10	10	30	10	10	10	10	10
焼成雰囲気	窒素雰囲気		窒素雰囲気			水素3%-窒素雰囲気		
低抵抗 (mΩ)	60	80	70	30	10	60	20	10
TCR (ppm/℃)	15	40	-20	30	40	-30	20	50
熱衝撃試験 -40℃~ +85℃ 500サイクル	±4%	±5%	±0.4%	±0.2%	±0.1%	±0.4%	±0.2%	±0.1%
高温放置 (150℃- 1000時間)	±5%	±6%	±0.7%	±0.3%	±0.2%	±0.6%	±0.3%	±0.2%

[0043] According to the gestalt of the 3rd operation, it has very low resistance, the resistor which was very excellent also in the thermal shock property and the heat-resistant long-term reliability trial is obtained, and the dependability of various electrical properties is also excellent so that clearly from (Table 3).

[0044] The resistor produced with the conventional method as an example of a comparison showed the inadequate engine performance from a viewpoint of heat-resistant long-term dependability.

[0045] Since it has the interface by which the top-face electrode layer and the resistive layer were alloyed, while having the low resistance and the low TCR property that electrode structure stable in heat-resistant property is acquired and realizing very few highly precise chip resistors of a change in resistance in heat-resistant long-term dependability according to the gestalten 1-3 of operation as mentioned above, the advantageous effectiveness that a resistor can be manufactured cheaply is acquired.

[0046] In addition, the thick film resistor constituent of the gestalten 1-3 of operation is baking in an elevated temperature [ semantics / which lowers resistance ] (600-1000 degrees C), and one sort of the high-melting glass frit whose glass transition point is 450-800 degrees C especially lead borosilicate textile glass yarn, and borosilicate zinc textile glass yarn, or two sorts or more are suitable for a glass frit. Although the value whose temperature coefficient of resistance is generally \*\*400 ppm/degree C since the direction near zero is desirable was chosen from viewpoints, such as engine performance and a price, the thing near 10 times was obtained by the price and the engine-performance ratio according to the gestalt of this operation.

[0047] Moreover, the substrate of a glass ceramic system besides an alumina, forsterite, a mullite, and aluminum nitride can use it widely that what is necessary is just what can bear the burning temperature of 600-1000 degrees C as an ingredient of a substrate.

[0048] (Gestalt 4 of operation) Drawing 4 is the cross section of the chip resistor in the gestalt of operation of the 4th of this invention. In drawing, 3 is a resistive layer and is carrying out printing

formation with thick-film formation techniques, such as screen-stencil, using the resistive paste which consists of an alloy presentation as shown in (Table 4) to both sides of the rectangular ceramic substrate (it is only hereafter called a substrate) 1. Next, printing formation of the top-face electrode layer 2 is carried out by the same approach as a resistive layer 3 so that field contact may be carried out with a resistive layer 3 to the both ends of this resistive layer 3, the end-face electrode layer 5 of the shape of a KO character of a pair is formed so that a part of top-face electrode layer 2 may be further covered at least to the both-sides side of a substrate 1, and coincidence baking of these is carried out in neutral atmosphere or reducing atmosphere.

[0049] Below, the production approach of resistive paste is shown. The copper-nickel system alloy powder used as the inorganic composition the mixed fine particles which added glass to this using the atomizing powder with a mean particle diameter of 2 micrometers. Moreover, this was made into the organic composition at the vehicle using what melted the ethyl cellulose which is an organic binder by terpeneol. These inorganic compositions and organic compositions were kneaded with 3 rolls, and it considered as the resistive paste which forms a resistive layer 3.

[0050] Next, the production approach of the electrode paste which forms the top-face electrode layer 2 is shown. Copper powder made this the inorganic composition using powder with a mean particle diameter of 2 micrometers. Moreover, this was made into the organic composition at the vehicle using what melted the ethyl cellulose which is an organic binder by terpeneol. These inorganic compositions and organic compositions were kneaded with 3 rolls, and it considered as the electrode paste for top-face electrode layer 2.

[0051] Below, the production approach of a chip resistor is shown. First, the resistive paste for resistive layer 3 was printed to both sides of a substrate 1 (6.4x3.2mm of 96% alumina substrates), and was dried for 10 minutes at the temperature of 100 degrees C. Next, it screen-stenciled and the top face of a resistive layer 3 was made to dry the electrode paste for top-face electrode layer 2 so that it may become the structure which carries out field contact. Subsequently, it applied so that it might become about 50-100 micrometers of thickness to an end face using commercial copper electrode paste as an end-face electrode layer 5, and these were calcinated for -10 minutes 900 degrees C in nitrogen-gas-atmosphere mind after that, and a chip resistor like drawing 4 was produced.

[0052] Below, the evaluation approach of a chip resistor is shown. Electrode distance between the top-face electrode layers 2 of a chip resistor was set to 4.0mm, the film width of a baking resistor was formed by 2.5mm, the probe was fixed to the top-face electrode layer 2, and the resistance between terminals was calculated by 4 terminal method. Moreover, the TCR property put the chip resistor into the thermostat, measured the resistance of 25 degrees C and 125 degrees C, and asked for the rate of change. The change in resistance in elevated-temperature neglect asked for the rate of a change in resistance when leaving resin at a coat (about 50 micrometers of thickness), and 160 degrees C for 1000 hours as a protective layer 11 as shown in a baking resistor drawing 10 and 11.

[0053] Structure was clarified for the cross-section section of the produced chip resistor using the scanning electron microscope, the electron probe microanalyzer, and the X-ray microdiffraction meter.

[0054] A result is shown in (Table 4).

[0055]

[Table 4]

No.	抵抗体組成 (wt %) Cu : Ni : Mn : Cr : Fe	上面抵抗体膜厚 ( $\mu$ m)	裏面抵抗体膜厚 ( $\mu$ m)	端子間抵抗値 (m $\Omega$ )	TCR (ppm/ $^{\circ}$ C)	高温放置 変化率 (%)
1	70 : 30 : 0 : 0 : 0	30	100	5.0	80	2.0
2	70 : 29 : 1 : 0 : 0	30	100	5.2	65	2.0
3	70 : 29 : 0 : 1 : 0	30	100	5.1	70	2.5
4	70 : 29 : 0 : 0 : 1	30	100	5.5	60	3.0

[900 $^{\circ}$ C-10min焼成]

[0056] According to the chip resistor of the gestalt of this operation, the chip resistor of low resistance, low TCR, and high-reliability is obtained by forming a resistive layer in both sides, and since the baking

particle diameter of a resistor layer is 40 micrometers or less and thickness is moreover 30 micrometers or less, trimming by the YAG laser can be performed so that more clearly than (Table 4). Since the energy of laser will be reflected if it is generally a metallic foil and a metal wire, laser trimming cannot be performed, and easy moreover by trimmings, such as sandblasting, highly precise trimming cannot be performed, but the chip resistor of the gestalt of this operation is very effective.

[0057] (Gestalt 5 of operation) Drawing 5 is the cross section of the chip resistor in the gestalt of operation of the 5th of this invention. In drawing, 3 is a resistive layer and 8 is the metallic foil 8 (mm [ 6.4x3.2 ], thickness = 0.04mm) which consists of an alloy presentation as shown in (Table 5).

[0058] In addition, production of the resistive paste for resistive layer 3 was performed by the same approach as the gestalt 4 of operation.

[0059] Below, the production approach of a chip resistor is shown. After printing the resistive paste which forms a resistive layer 3 first on the metallic foil 8 and drying it for 10 minutes at the temperature of 100 degrees C, 900 degrees C was calcinated for -10 minutes in nitrogen-gas-atmosphere mind, and a chip resistor like drawing 5 was produced.

[0060] About the evaluation approach of a chip resistor, it carries out by the same approach as the gestalt 4 of operation, and the result is shown in (Table 5).

[0061]

[Table 5]

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属箔組成 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu$ m)	端子間抵抗値 (m $\Omega$ )	TCR (ppm/ $^{\circ}$ C)	高温放置 変化率 (%)
5	70:30: 0: 0: 0	70:30: 0: 0	30	3.0	80	2.0
6	70:30: 0: 0: 0	70:29: 1: 0	30	4.0	65	2.0
7	70:30: 0: 0: 0	0:95: 5: 0	30	3.4	70	2.6
8	70:30: 0: 0: 1	0:95: 4: 1	30	3.5	60	3.0

[900 $^{\circ}$ C-10min焼成]

[0062] (Gestalt 6 of operation) Drawing 6 is the cross section of the chip resistor in the gestalt of operation of the 6th of this invention. In drawing, 3 is a resistive layer, and 8 is a metallic foil as shown in (Table 6), and is carrying out printing formation with thick-film formation techniques, such as screen-stencil, using the resistive paste which consists of an alloy presentation as shown in (Table 6) to both sides of the rectangular substrate 1. Next, printing formation of the top-face electrode layer 2 is carried out by the same approach as a resistive layer 3 so that field contact may be carried out with a resistive layer 3 to the both ends of this resistive layer 3, the end-face electrode layer 5 of the shape of a KO character of a pair is formed, and coincidence baking of these is carried out in neutral atmosphere or reducing atmosphere so that a part of top-face electrode layer 2 may be further covered at least to the both-sides side of a substrate 1.

[0063] In addition, about production of the resistive paste for resistive layer 3, and production of the electrode paste for top-face electrode layer 2, it carried out by the same approach as the gestalt 4 of operation.

[0064] Below, the production approach of a chip resistor is shown. The metallic foil 8 (mm [ 3.8x2.3 ], thickness = 0.02mm) was made to fix by adhesion etc. first on a substrate 1 (6.4x3.2mm of 96% alumina substrates), the resistive paste which forms a resistive layer 3 on it was printed, and it was made to dry for 10 minutes at the temperature of 100 degrees C. Next, it screen-stenciled and the top face of a resistive layer 3 was made to dry the electrode paste which forms the top-face electrode layer 2 so that it may become the structure which carries out field contact. Next, it applied so that it might become about 50-100 micrometers of thickness to an end face using commercial copper electrode paste as an end-face electrode layer 5, and these were calcinated for -10 minutes 900 degrees C in nitrogen-gas-atmosphere mind after that, and a chip resistor like drawing 6 was produced.

[0065] About the evaluation approach of a chip resistor, it carries out by the same approach as the gestalt 4 of operation, and the result is shown in (Table 6).

[0066]

[Table 6]

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属箔組成表 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
9	70:30:0:0:0	70:30:0:0:0	30	4.0	80	2.0
10	70:30:0:0:0	70:29:1:0:0	30	5.0	65	2.0
11	70:30:0:0:0	0:95:5:0:0	30	4.4	70	2.6
12	70:30:0:0:1	0:95:4:1:0	30	4.5	60	3.0

[900 $^\circ\text{C}$ -10min焼成]

[0067] (Gestalt 7 of operation) Drawing 7 is cross section \*\*\*\* of the chip resistor in the gestalt of operation of the 7th of this invention.

[0068] In addition, the gestalt of this operation is replaced with the metallic foil 8 of the gestalt of the 6th operation, shows the example using the metal wire 9 as shown in (Table 7), and it is constituted so that the slit (not shown) prepared on the substrate 1 may be fitted in and loaded, using a thing (diameter = 0.6mm and die-length = 3.8mm) as a metal wire 9.

[0069] About the evaluation approach of a chip resistor, it carries out by the same approach as the gestalt 4 of operation, and the result is shown in (Table 7).

[0070]

[Table 7]

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属箔組成表 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
13	70:30:0:0:0	70:30:0:0:0	30	2.0	80	2.0
14	70:30:0:0:0	70:29:1:0:0	30	2.5	65	2.0
15	70:30:0:0:0	0:95:5:0:0	30	2.2	70	2.6
16	70:30:0:0:1	0:95:4:1:0	30	2.3	60	3.0

[900 $^\circ\text{C}$ -10min焼成]

[0071] (Gestalt 8 of operation) Drawing 8 is the cross section of the chip resistor in the gestalt of operation of the 8th of this invention. In drawing, 3 is a resistive layer, and 8 is a metallic foil as shown in (Table 8), and is carrying out printing formation with thick-film formation techniques, such as screen-stencil, using the resistive paste which becomes another one side of the rectangular substrate 1 from an alloy presentation as shown in (Table 8). Next, printing formation of the top-face electrode layer 2 is carried out by the same approach as a resistive layer 3 so that field contact may be carried out with a resistive layer 3 to the both ends of this resistive layer 3, the end-face electrode layer 5 of the shape of a KO character of a pair is formed so that a part of top-face electrode layer 2 may be further covered at least to the both-sides side of a substrate 1, and coincidence baking of these is carried out in neutral atmosphere or reducing atmosphere.

[0072] In addition, about production of the resistive paste for resistive layer 3, and production of the electrode paste for top-face electrode layer 2, it carried out by the same approach as the gestalt 4 of operation.

[0073] The production approach of a chip resistor is shown below. A metallic foil 8 (mm [ 6.4x2.5 ], thickness = 0.1mm) is first fixed to one side of a substrate 1 (6.4x3.2mm of 96% alumina substrates) by adhesion etc., and the resistive paste which forms a resistive layer 3 was printed to the field where a metallic foil 8 is opposite, and was dried for 10 minutes at the temperature of 100 degrees C. Next, screen-stencil formation was carried out and the top face of a resistive layer 3 was made to dry the electrode paste which forms the top-face electrode layer 2 so that it may become the structure which carries out field contact. Subsequently, it applied so that it might become about 50-100 micrometers of thickness to an end face using commercial copper electrode paste as an end-face electrode layer 5, and after that, these were calcinated for -10 minutes 900 degrees C in nitrogen-gas-atmosphere mind, and a chip resistor like drawing 8 was produced.

[0074] About the evaluation approach of a chip resistor, it carries out by the same approach as the

gestalt 4 of operation, and the result is shown in (Table 8).

[0075]

[Table 8]

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属線組成 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
17	70:30: 0: 0: 0	70:30: 0: 0	30	1.0	100	2.0
18	70:30: 0: 0: 0	70:29: 1: 0	30	1.2	85	2.0
19	70:30: 0: 0: 0	0:95: 5: 0	30	1.1	80	2.6
20	70:30: 0: 0: 1	0:95: 4: 1	30	1.0	80	3.0

[900 $^\circ\text{C}$ -10min焼成]

[0076] (Gestalt 9 of operation) Drawing 9 is the cross section of the chip resistor in the gestalt of operation of the 9th of this invention. In drawing, 3 is a resistive layer, and 9 is a metal wire as shown in (Table 9), and is carrying out printing formation with thick-film formation techniques, such as screen-stencil, using the resistive paste which consists of an alloy presentation as shown in (Table 8) to both sides of the rectangular substrate 1. Next, printing formation of the top-face electrode layer 2 is carried out by the same approach as a resistive layer 3 so that field contact may be carried out with a resistive layer 3 to the both ends of this resistive layer 3, the end-face electrode layer 5 of the shape of a KO character of a pair is formed so that a part of top-face electrode layer 2 further prepared in the both-sides side of a substrate 1 to both sides at least may be covered, and coincidence baking of these is carried out in neutral atmosphere or reducing atmosphere.

[0077] In addition, about production of the resistive paste for resistive layer 3, and production of the electrode paste for top-face electrode layer 2, it carried out by the same approach as the gestalt 4 of operation.

[0078] Below, the production approach of a chip resistor is shown. Insertion immobilization of the metal wire 9 (diameter = 0.6mm, die length = 3.8mm) is carried out at the slit (not shown) first prepared in one side of a substrate 1 (6.4x3.2mm of 96% alumina substrates). Next, the resistive paste which forms a resistive layer 3 was printed to the both sides, and was dried for 10 minutes at the temperature of 100 degrees C. Next, screen-stencil formation was carried out and the top face of both the resistive layers 3 was made to dry the electrode paste which forms the top-face electrode layer 2 so that it may become the structure which carries out field contact. Subsequently, it applied so that it might become about 50-100 micrometers of thickness to an end face using commercial copper electrode paste as an end-face electrode layer 5, and after that, these were calcinated for -10 minutes 900 degrees C in nitrogen-gas-atmosphere mind, and a chip resistor like drawing 9 was produced.

[0079] About the evaluation approach of a chip resistor, it carries out by the same approach as the gestalt 4 of operation, and the result is shown in (Table 9).

[0080]

[Table 9]

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属線組成 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
21	70:30: 0: 0: 0	70:30: 0: 0	30	1.5	80	2.0
22	70:30: 0: 0: 0	70:29: 1: 0	30	1.7	65	2.0
23	70:30: 0: 0: 0	0:95: 5: 0	30	1.6	70	2.6
24	70:30: 0: 0: 1	0:95: 4: 1	30	1.5	60	3.0

[900 $^\circ\text{C}$ -10min焼成]

[0081] In addition, although the gestalten 4-9 of operation showed the example which takes the flow of an upper rear-face resistor as an end-face electrode layer 5, it is also possible to form a through hole etc. in a substrate 1, to make it bury and flow through a metal paste metallurgy group, and to form a low resistor chip resistor. Moreover, while being able to save time and effort, such as adhesion, if irregularity (slit) is given to a substrate 1, a metallic foil and a metal wire are fixed to a crevice and a resistor is



formed when using a metallic foil or a metal wire, they can certainly be fixed, without using matter which affects the property included in adhesives, and it is very effective.

[0082] Moreover, although the gestalt of this operation explained the example of the trimming by the YAG laser, even if it performs trimming by other laser, it is found out experimentally that the case where baking particle diameter is especially 40 micrometers or less, and thickness is 30 micrometers or less is [ that that the same effectiveness is acquired should just form the thickness of a resistor layer in the range in which the trimming by the laser to say is possible needless to say ] desirable.

[0083]

[Effect of the Invention] As mentioned above, according to this invention, since junction of a resistive layer and a top-face electrode layer is performed by metal junction, the chip resistor which was excellent in the high-reliability which it is not placed between the interfaces by impurity which affects a property, has the low resistance and the low TCR property of having fully employed the material property of copper/nickel alloy efficiently, and was excellent in the heat-resistant property is realizable.

[0084] Moreover, since it is constituted so that it may be 30 micrometers or less and the thickness may be set to 40 micrometers or less in the sintering particle diameter of a baking resistor layer, the trimming by laser becomes possible, it becomes possible to perform trimming with a sufficient precision very easy moreover compared with polishing by sandblasting etc., and a very cheap and highly precise chip resistor can be realized.

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[Translation done.]

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松下電器産業株式会社

大阪府門真市大字門真1006番地

(31) 優先権主張番号 特願平8-240294

(72) 発明者 下山 浩司

大阪府門真市大字門真1006番地 松下電器  
産業株式会社内

(32) 優先日 平8(1996) 9月11日

(72) 発明者 中尾 恵一

大阪府門真市大字門真1006番地 松下電器  
産業株式会社内

(33) 優先権主張国 日本 (J P)

(72) 発明者 木村 涼

大阪府門真市大字門真1006番地 松下電器  
産業株式会社内

(74) 代理人 弁理士 滝本 智之 (外1名)

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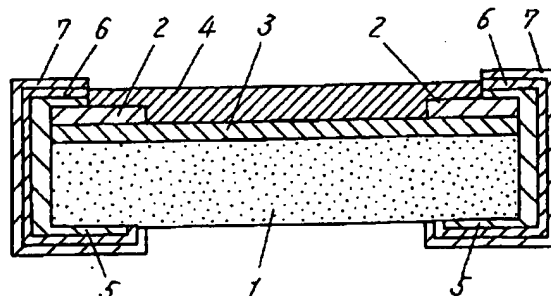
(54) 【発明の名称】 チップ抵抗器及びその製造方法

(57) 【要約】

【課題】 各種電気機器回路部品に使用されるチップ抵抗器に関し、低抵抗、低TCR特性を実現するとともに、高精度、高信頼性を実現することを目的とする。

【解決手段】 基板1と、この基板1の少なくとも片面に形成した銅／ニッケル合金からなる抵抗層3と、この抵抗層3の両端部を上面から面接触するように形成された上面電極層2と、この上面電極層2を覆うように設けられた端面電極層5とを有する構成に形成しており、特に、抵抗層3と上面電極層5の接合が金属接合であるため、界面には特性に影響を与えるような不純物が介在せず、耐熱性に優れた低抵抗、低TCR特性のチップ抵抗器が実現できる。

- 1 基 板
- 2 上面電極層
- 3 抵抗層
- 4 保護膜層
- 5 端面電極層
- 6 Niめっき膜
- 7 はんだめっき膜



## 【特許請求の範囲】

【請求項1】 絶縁基板と、この絶縁基板の少なくとも片面に設けられた銅／ニッケル合金粉およびガラスフリットからなる抵抗層と、この抵抗層の両端部にそれぞれ上面から面接触するように設けられた一対の上面電極層と、この上面電極層の少なくとも一部を覆うように前記絶縁基板の両側面に設けられた一対の端面電極とを備え、前記抵抗層と前記上面電極層との接合が金属接合であることを特徴とするチップ抵抗器。

【請求項2】 上面電極層の抵抗値が抵抗層より低いことを特徴とする請求項1記載のチップ抵抗器。

【請求項3】 上面電極層が銅電極または銀電極からなることを特徴とする請求項2記載のチップ抵抗器。

【請求項4】 絶縁基板と、この絶縁基板の少なくとも片面の両端部に設けられた一対の下面電極層と、この一対の下面電極層をつなぐように設けられた銅／ニッケル合金粉およびガラスフリットからなる抵抗層と、この抵抗層の前記下面電極層と対向する両端部にそれぞれ上面から面接触するように設けられた一対の上面電極層と、この上面電極層の少なくとも一部を覆うように前記絶縁基板の両側面に設けられた一対の端面電極とを備え、前記抵抗層と前記上面電極層との接合が金属接合であることを特徴とするチップ抵抗器。

【請求項5】 上面電極層および下面電極層の抵抗値が抵抗層より低いことを特徴とする請求項4記載のチップ抵抗器。

【請求項6】 上面電極層および下面電極層が銅電極または銀電極からなることを特徴とする請求項4記載のチップ抵抗器。

【請求項7】 絶縁基板の少なくとも片面に銅／ニッケル合金粉およびガラスフリットからなる抵抗層を形成する工程と、この抵抗層の両端部にそれぞれ上面から面接触するように一対の上面電極層を形成し、焼成する工程と、焼結形成された上面電極層の少なくとも一部を覆うように前記絶縁基板の両側面に一対の端面電極を形成する工程とを有し、焼結形成された抵抗層と上面電極層とが金属接合により接合されていることを特徴とするチップ抵抗器の製造方法。

【請求項8】 抵抗層および上面電極層を窒素雰囲気下でまたは水素を含んだ還元雰囲気下で600～1000℃の温度で焼結形成することを特徴とする請求項7記載のチップ抵抗器の製造方法。

【請求項9】 絶縁基板の少なくとも片面の両端部に一対の下面電極層を形成する工程と、この一対の下面電極層をつなぐように銅／ニッケル合金粉およびガラスフリットからなる抵抗層を形成する工程と、この抵抗層の両端部にそれぞれ上面から面接触するように一対の上面電極層を形成し、焼成する工程と、焼結形成された上面電極層の少なくとも一部を覆うように前記絶縁基板の両側面に一対の端面電極を形成する工程とを有し、焼結形成

された下面電極層と抵抗層および抵抗層と上面電極層とがそれぞれ金属接合により接合されていることを特徴とするチップ抵抗器の製造方法。

【請求項10】 抵抗層および上面電極層を窒素雰囲気下でまたは水素を含んだ還元雰囲気下で600～1000℃の温度で焼結形成することを特徴とする請求項9記載のチップ抵抗器の製造方法。

【請求項11】 セラミック基板の両面に設けられ少なくとも銅／ニッケル合金粉末からなる焼結形成された焼成抵抗体層と、この両面の焼成抵抗体層のそれぞれの両端部の一部を少なくとも覆うように設けられた端子電極と、この端子電極のそれぞれの両端部の一部を少なくとも覆うように前記セラミック基板の両側面に設けられた端面電極とを備え、前記セラミック基板の少なくとも片面に設けられた焼成抵抗体層の焼結粒子径が30μm以下で、かつその膜厚が40μm以下であることを特徴とするチップ抵抗器。

【請求項12】 少なくとも銅／ニッケルまたはニッケル／クロムからなる金属箔と、この金属箔上に設けられ少なくとも銅／ニッケルからなる焼結形成された焼成抵抗体層とを備え、前記焼成抵抗体層の焼結粒子径が30μm以下で、かつその膜厚が40μm以下であることを特徴とするチップ抵抗器。

【請求項13】 セラミック基板の少なくとも片面に設けられた少なくとも銅／ニッケルまたはニッケル／クロムからなる金属箔と、この金属箔上に設けられ少なくとも銅／ニッケルからなる焼結形成された焼成抵抗体層と、この焼成抵抗体層のそれぞれの両端部の一部を少なくとも覆うように設けられた一対の端子電極と、この端子電極のそれぞれの両端部の一部を少なくとも覆うように前記セラミック基板の両側面に設けられた端面電極とを備え、前記焼成抵抗体層の焼結粒子径が30μm以下で、かつその膜厚が40μm以下であることを特徴とするチップ抵抗器。

【請求項14】 金属箔に代え少なくとも銅／ニッケルまたはニッケル／クロムからなる金属線を用いたことを特徴とする請求項13記載のチップ抵抗器。

【請求項15】 セラミック基板の片面に設けられた少なくとも銅／ニッケルまたはニッケル／クロムからなる金属箔と、もう一方の片面に設けられ少なくとも銅／ニッケルからなる焼結形成された焼成抵抗体層と、この焼成抵抗体層のそれぞれの両端部の一部を少なくとも覆うように設けられた一対の端子電極と、この端子電極のそれぞれの両端部の一部および金属箔の両端部の一部を少なくとも覆うように前記セラミック基板の両側面に設けられた端面電極とを備え、前記焼成抵抗体層の焼結粒子径が30μm以下で、かつその膜厚が40μm以下であることを特徴とするチップ抵抗器。

【請求項16】 セラミック基板の片面に設けられた少なくとも銅／ニッケルまたはニッケル／クロムからなる

金属線と、もう一方の片面および前記金属線の上面に設けられ少なくとも銅／ニッケルからなる焼結形成された焼成抵抗体層と、この両面の焼成抵抗体層のそれぞれの両端部の一部を少なくとも覆うように設けられた端子電極と、この端子電極のそれぞれの両端部の一部を少なくとも覆うように前記セラミック基板の両側面に設けられた端面電極とを備え、前記2つの焼成抵抗体層の少なくとも一方の焼結粒子径が $30\mu\text{m}$ 以下で、かつその膜厚が $40\mu\text{m}$ 以下であることを特徴とするチップ抵抗器。

【請求項17】 その端面電極の少なくとも一部を残して樹脂でその全体を覆うことを特徴とする請求項11～16のいずれかに記載されたチップ抵抗器。

【請求項18】 セラミック基板の両面に少なくとも銅／ニッケル合金粉末からなる抵抗体層を形成する工程と、この抵抗体層のそれぞれの両端部の一部を少なくとも覆うように端子電極を形成する工程と、この端子電極のそれぞれの両端部の一部を少なくとも覆うように前記セラミック基板の両側面に端面電極を形成後、これを焼成する工程と、この焼成された抵抗体をトリミングする工程とを備え、前記セラミック基板の少なくとも片面に設けられた抵抗体層の膜厚をレーザーによるトリミングが行える膜厚範囲内に形成したことを特徴とするチップ抵抗器の製造方法。

【請求項19】 少なくとも銅／ニッケルまたはニッケル／クロムからなる金属箔上に、少なくとも銅／ニッケルからなる抵抗体層を形成し、焼成後トリミングを行う際に、抵抗体層の膜厚をレーザーによるトリミングが行える膜厚範囲内に形成したことを特徴とするチップ抵抗器の製造方法。

【請求項20】 セラミック基板の少なくとも片面に少なくとも銅／ニッケルまたはニッケル／クロムからなる金属箔または金属線を形成する工程と、この金属箔または金属線上に少なくとも銅／ニッケルからなる抵抗体層を形成する工程と、この抵抗体層の両端部の一部を少なくとも覆うように一対の端子電極を形成する工程と、この端子電極のそれぞれの両端部の一部および金属箔または金属線の両端部の一部を少なくとも覆うように前記セラミック基板の両側面に端面電極を形成後、これを焼成する工程と、この焼成された抵抗体をトリミングする工程とを備え、前記セラミック基板の少なくとも片面に設けられた抵抗体層の膜厚をレーザーによるトリミングが行える膜厚範囲内に形成したことを特徴とするチップ抵抗器の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は電子回路に広く使われるチップ抵抗器に関し、特に低抵抗、低TCR特性を有するチップ抵抗器およびその製造方法に関するものである。

【0002】

【従来の技術】近年、携帯電話、ムービー、ノートパソコンなどに代表されるように、小型電子機器の需要は高まる一方であり、今後これらの電子機器の小型化、高性能化はこれに用いられるチップ型電子部品の小型化、高性能化に依存していると言って過言でない。厚膜抵抗体としては酸化ルテニウムおよびその複合酸化物であるルテニウム酸ビスマスやルテニウム酸鉛を主成分とする組成物が知られており（例えば、特公昭58-37963号公報参照）、種々の分野で利用されている。

10 【0003】従来のチップ抵抗器の製造方法の一例について図面に基づいて説明する。図12は、従来の角形チップ抵抗器の構造の一例を示す斜視図であり、図13は図12のA-A'部における断面図である。一般にこの種の角形チップ抵抗器の製造方法は、まず、96%アルミナからなるチップ状のアルミナ基板10の上面に、上部電極11を形成し、次にアルミナ基板10の上面の一部に、上記上部電極と接続するように抵抗体12を形成し、さらにこの抵抗体12を完全に覆うように、ホウケイ酸鉛系ガラスからなる保護膜14を形成している。一般的には、上記保護膜14は、スクリーン印刷によりパターン形成を行った後、 $500\sim 800^{\circ}\text{C}$ という高温で焼成する事により形成される。

20 【0004】次に上記アルミナ基板10の端面部に、上部電極11とを接続するようにAg系の厚膜でなる端面電極13を形成し、このときこの端面電極13は、一般に $600^{\circ}\text{C}$ 付近の高温で焼成する事により形成される。最後に、はんだ付けを行うときの信頼性を確保するために、上記端面電極13を覆うようにNiめっき膜15を電気めっきにより形成し、そしてはんだめっき膜16をこのNiめっき膜15を覆うように形成して角形チップ抵抗器を得ている。

【0005】上記のような製造方法にて製造されるチップ抵抗器においては、一般に、抵抗体となる導電粒子として酸化ルテニウムを主成分とする厚膜グレース抵抗体材料が用いられるが、この酸化ルテニウムのみからなる抵抗体材料では、抵抗値の温度変化を示す抵抗温度係数（以下、TCRという）が大きくなるため、金属酸化物などのTCR調整材を添加することにより $\pm 50\text{ppm}/^{\circ}\text{C}$ 程度以内という低い値にして用いる必要があった。

40 【0006】しかし、このような抵抗体材料を用いた場合、酸化ルテニウムの比抵抗が高いために、 $1\Omega$ 以下の低い抵抗値を有するチップ抵抗器を形成することが困難であった。そのため、 $1\Omega$ 以下の低抵抗体材料としてJIS C2521や同C2532に記載されているような抵抗温度係数の小さい銅／ニッケル合金を用いたチップ抵抗器が提案されている。

50 【0007】すなわち、この合金材料を箔または板の形状に加工してアルミナ基板上に張りつける構造や、銅粉、ニッケル粉そしてガラスフリットを有機ビヒクルにて混練した抵抗体ペーストをアルミナ基板上に印刷した

後、不活性雰囲気中にて焼成する事によって合金膜を形成する構造のものが提案されている(特開平2-308501号公報、特開平3-270104号公報参照)。

【0008】

【発明が解決しようとする課題】しかしながら、前者の場合、合金箔或いは合金板を加工する方法は、チップ部品の形状が益々小型化の方向に進んでいる中で限界があり、またトリミングはレーザーを用いることができず、研磨等では限界があり、さらにコスト的にも印刷方法に比較して不利であるため、あまり量産性に優れたものではなかった。

【0009】また、後者の場合、抵抗体膜と基板の接着や抵抗値の調整にガラスを用いており、銅、ニッケル以外の成分が多く含まれていることから、温度係数が銅-ニッケル合金の物性値と異なってくるとともに、ガラス成分は焼成条件によって金属成分中や焼結粒子界面への拡散挙動が異なるために、安定した抵抗値特性が得られにくいという課題を有していた。

【0010】さらに、銅、ニッケル粉を用いたペースト法では、給電部の端子電極の特性や抵抗体/電極界面の構造が抵抗器としての特性を大きく左右するため、抵抗値としては100mΩまでが限界であり、さらに低い抵抗値を実現することは困難であった。

【0011】前述のごとく、近年、チップ抵抗器の形状は益々小型化の傾向となる一方、電子回路の電流検出などに用いられる低抵抗でかつ、低TCR特性を有するチップ抵抗器の要望が益々高まっており、更に用いられる用途の性能から、低抵抗、低TCR特性に加え、高精度、高信頼性をも満足するようなチップ抵抗器が切望されている。

【0012】本発明は、上述した課題を解決し、上記要望に応えるものであり、1Ω以下、特に100mΩ以下の低抵抗、低TCR特性を持ち、かつ高信頼性を有するチップ抵抗器及びその製造方法を提供することを目的とする。

【0013】

【課題を解決するための手段】本発明は、絶縁基板と、この絶縁基板の少なくとも片面に形成された銅/ニッケル合金からなる抵抗層と、この抵抗層の両端部のそれぞれを上面から面接触するように形成された一対の上面電極層と、この上面電極層の少なくとも一部を覆うように前記絶縁基板の両端部に形成された一対の端面電極とを有するチップ抵抗器であり、特に、抵抗層と上面電極層の接合が金属接合で行われているため、界面には特性に影響を与えるような不純物が介在せず、低抵抗、低TCR特性でかつ耐熱性に優れたチップ抵抗器が得られる。

【0014】

【発明の実施の形態】

(実施の形態1) 図1は本発明の第1の実施の形態におけるチップ抵抗器の断面模式図を示す。図において、3

は抵抗層であり、方形の絶縁基板(以下、単に基板と呼ぶ)1の片面に、(表1)に示すような合金組成よりなる抵抗体ペーストを用いてスクリーン印刷などの厚膜技術により印刷形成している。次に基板1に対向する一対の両端部に抵抗層3と面接触するように上面電極層2を抵抗層3と同じ方法で印刷形成し、この抵抗層3と上面電極層2とを中性雰囲気もしくは還元雰囲気中にて同時焼成している。その後、この抵抗層3の一部を覆うように保護膜層4を形成し、また基板1の対向する一対の両端部にコ字状かつ、抵抗層3の保護膜層4で覆われていない部分に端面電極層5を形成している。さらにこの端面電極層5を覆うNiめっき膜6を形成し、このNiめっき膜6上にはんだめっき膜7を形成している。

【0015】以下に、チップ抵抗器の作製方法について詳述する。抵抗体ペーストは銅/ニッケル合金粉(平均粒子径5μmのアトマイズ粉)を用い、これにガラスフリットを添加した混合粉体を無機組成物とした。ガラスフリットは硼珪酸鉛ガラスを金属粉に対して5重量%の割合にて添加し、また、ビヒクル成分には有機バインダであるエチルセルロースをタービネオールで溶かしたものをを用い、これを有機ビヒクル組成物とした。これらの無機組成物と有機ビヒクル組成物を三本ロールにて混練し抵抗体ペーストとした。

【0016】次に、上面電極ペーストは銅粉(平均粒子径:2μm)または銀粉(平均粒子径:5μm)を用い、ビヒクル成分には有機バインダであるエチルセルロースをタービネオールで溶かしたものをを用い、これを有機ビヒクル組成物とした。これらの無機組成物と有機ビヒクル組成物を三本ロールにて混練し上面電極ペーストとした。

【0017】このようにして調整した前記抵抗体ペーストをスクリーン版を用いて基板1(96%アルミナ基板)上に抵抗体パターンを印刷し、100℃の温度で10分間乾燥させるとともに、続いて前記上面電極ペーストを抵抗体パターンの上面にスクリーン版を用いて図1に示すような所定のパターンに印刷し、100℃の温度で10分間乾燥させた。次にこの基板1を窒素雰囲気焼成のできるプロファイルにて抵抗体、電極の同時焼成を行って抵抗層3と上面電極層2を同時形成し、さらに基板1を分割して端面電極5として銅電極を設けた後、抵抗層3の保護膜としてエポキシ樹脂をスクリーン印刷にて保護膜層4を形成し、160℃、30分の条件にて樹脂硬化させた。できた抵抗体素子の抵抗値、抵抗値の温度係数(TCR)および信頼性(高温放置試験、熱衝撃試験)について評価した。

【0018】また、比較例として図13に示すような構造になるように上部電極11としてガラスフリットを含む銅電極あるいは銀電極を形成した後、合金粉とガラスと有機ビヒクルを前記と同様にペースト化したものをアルミナ基板10(96%アルミナ基板)上に印刷し、1

00℃の温度で10分間乾燥させた後、N<sub>2</sub>雰囲気下で（表1）に示す焼成条件にて加熱して抵抗体の焼成を行った。

【0019】次に焼成後の抵抗器の評価方法について示す。抵抗値は試料を温度25±2℃、湿度65±10% RHの雰囲気中に30分間以上静置したのち4端子法で求めた。また、TCR特性は抵抗器を恒温槽に入れ試料を温度雰囲気中に30分間以上静置したのち、25℃と125℃の抵抗値を測定しその変化率を求めた。

【0020】信頼性評価項目である熱衝撃試験はあらかじめ【表1】

\* じめ所定の温度に設定された2つの試験槽（-45℃、+150℃）があり、一つの試験槽に30分間保持した後すぐに、他方の試験槽に30分間曝される試験を500サイクル繰り返した後の抵抗値変化率を評価した。また、高温放置試験は150℃に保持された試験槽に1000時間放置した後の抵抗値変化率を評価した。

【0021】また作製した抵抗器の合金層断面部をX線回折装置を用いて結晶構造を明らかにした。

【0022】

合金組成 Cu/Ni (重量比)	比較例 70/30 +ガラスフリット5wt%		70/30 +ガラスフリット5wt%					
	銅粉+ ガラスフリット 5wt%	銀粉+ ガラスフリット 5wt%						
上部電極			銅電極			銀電極		
焼成温度 (℃)	900	850	600	900	1000	600	800	850
焼成時間 (時間)	10	10	30	10	10	10	10	10
抵抗値 (mΩ)	60	80	70	40	10	90	70	60
TCR (ppm/℃)	15	40	-10	10	20	-20	10	40
熱衝撃試験 -40℃～ +85℃ 500サイクル	±4%	±5%	±0.4%	±0.2%	±0.1%	±0.5%	±0.3%	±0.2%
高温放置 (150℃～ 1000時間)	±5%	±6%	±0.7%	±0.4%	±0.2%	±0.9%	±0.5%	±0.3%

【0023】（表1）の結果より、従来の構造にて作製された比較例の抵抗体膜は上部電極との接続が高精度、高信頼性を要求される抵抗体としての品質としては十分であることが分かる。その時の膜質を断面観察すると抵抗体12と上部電極11との界面においてガラスフリットの存在や空隙などが多くみられ、焼結による緻密化が十分に進んでいないことが分かった。

【0024】一方本発明方法にて作製された抵抗層3と上面電極層2の界面はガラスフリットを含んでいないために不純物が介在せず、また同時焼結によって上面電極層2と抵抗層3との金属拡散によって結合された明確な界面を持たない結晶構造が実現できていることが分かった。このことは同時焼結によって銅もしくは銀が抵抗層である銅/ニッケル合金層中に拡散することによってはっきりとした界面の無い拡散層を有することが信頼性面で優れた熱安定性を示すものと思われる。焼結後の金属膜をX線回折装置にて解析したところ均一な銅/ニッケル合金層を形成している事が分かった。さらに、膜質を走査型電子顕微鏡にて観察したところ空隙の殆ど無い緻密な焼結膜が得られていることが分かった。

【0025】次に図2の製造工程図に従ってこのチップ抵抗器の具体的な製造方法を説明する。

【0026】銅/ニッケル合金粉末とガラスフリットの

比率を変えた抵抗体組成物を三本ロールミルにより混合し、粘度20～25万パスカル・秒の抵抗体ペーストを調整した（Step1）。

【0027】このペーストをアルミナ基板にスクリーン印刷、乾燥（抵抗体サイズ：2mm角、乾燥膜厚：40μm）して抵抗体を形成し（Step2）、上面電極層として銅粉（平均粒子径：2μm）または銀粉（平均粒子径：5μm）と有機ビヒクルとを三本ロールミルにより混練し、粘度20～25万パスカル・秒の電極ペーストを調整した（Step3）。この電極ペーストを用いて図1に示すような前記抵抗体の上面に面接触する構造になるようにスクリーン印刷、乾燥形成（乾燥膜厚：30μm）する（Step4）。その後、窒素雰囲気下で900℃にて10分間保持して焼成し抵抗層3および上面電極層2を作製した（Step5）。

【0028】ついで端面電極として市販の銅電極ペーストを用いて端面に膜厚約50～100μmになるように塗布し、窒素雰囲気にて800℃にて10分間焼成して端面電極層5を形成した（Step6）。その後YAGレーザーにより抵抗層3を切断トリミングを行ない（Step7）、続いて保護膜としてエポキシ樹脂ペースト（Step8）を抵抗層上に印刷・硬化（硬化膜厚：40μm、150℃にて30分間硬化保持）して保護膜層4を作製

した(Step9)。

【0029】その後、チップ部品とするためにNiめっき6及びはんだめっき7を端面に処理することによって(Step10, 11)、実装時のはんだ濡れ性を高める設計を実施した。

【0030】このような製造方法にて得られた抵抗器は(表1)から明らかなように、高温放置、熱衝撃試験といった耐熱特性において十分な信頼性を有していることが分かる。高温において安定な理由としては金属層の界面を明確に持たないで、合金化された拡散層を有していることと、上面電極層に不純物であるガラスフリットを含まないために低抵抗、低TCR特性で耐熱性に優れたチップ抵抗器を実現できた。

【0031】また、一般的には銅/ニッケルの合金比率を変えることにより抵抗温度係数(TCR特性)は400~200ppm/°Cの範囲で調節可能であるが、本実施の形態1では焼成温度条件も含めて40~20ppm/°Cの範囲に抑えられ、また、抵抗値も10mΩまでの低抵抗値範囲までカバーできた。しかも、抵抗体として要求される接着強度も優れている。また、その他の信頼性評価においても実用上十分な抵抗体としての耐久性を有していた。

【0032】なお、保護膜として本実施の形態では樹脂\*

\*ペーストを用いたが、通常よく使われるガラスペーストを用いても同様の効果が得られることは言うまでもない。

【0033】(実施の形態2)以下に、(表2)に示す合金粉混合比組成のものを用いて、実施の形態1と同様の方法で調整した抵抗体ペーストを、(表2)に示す焼成雰囲気で実施の形態1と同様に印刷焼成して得られたチップ抵抗器について説明する。

【0034】このようにして作製したチップ抵抗器の抵抗値、抵抗値の温度係数(TCR)、信頼性(高温放置、熱衝撃試験)について評価した。

【0035】また、比較例として図13に示すような上部電極11が形成された基板10上に合金粉とガラスフリットと有機ビヒクルを実施の形態1と同様にペースト化したものをスクリーン版を用いて印刷し、100°Cの温度で10分間乾燥させた後、N<sub>2</sub>雰囲気下で1000°Cに加熱して抵抗体の焼成を行った。その後、実施の形態1と同様に端面電極、保護膜を形成し抵抗器とした。

【0036】焼成後の抵抗器の評価方法も実施の形態1と同様の方法で求めた。その結果を(表2)に示す。

【0037】

【表2】

合金組成 Cu/Ni (重量比)	比較例 40/60 +ガラスフリット3 wt%		40/60 +ガラスフリット3 wt%					
上部電極	銅粉+ ガラスフリット 5wt%	銀粉+ ガラスフリット 4 wt%						
上面電極			銅電極			銀電極		
焼成雰囲気	水素1%—酸素雰囲気 (還元雰囲気)							
焼成温度 (℃)	900	850	600	900	1000	600	800	850
焼成時間 (時間)	10	10	30	10	10	10	10	10
抵抗値 (mΩ)	50	70	60	30	10	80	60	50
TCR (ppm/℃)	35	50	-30	20	15	-15	10	30
熱衝撃試験 -40℃~ +85℃ 500サイクル	±5%	±6%	±0.7%	±0.3%	±0.2%	±0.6%	±0.5%	±0.3%
高温放置 (150℃— 1000時間)	±6%	±7%	±0.5%	±0.3%	±0.2%	±0.8%	±0.4%	±0.3%

【0038】(表2)から明らかなように、本実施の形態方法にて作製された抵抗層3と上面電極層2の界面は不純物が介在せず、また同時焼結によって上面電極層2と抵抗層3との金属拡散によって結合された明確な界面を持たない結晶構造が実現できている。このことは同時焼結によって界面の無い拡散層を有することが信頼性面で優れた熱安定性を示すものである。これらのことよ

り、低抵抗、低TCR特性を有し、信頼性に優れた特性を示すチップ抵抗器が得られることが分かる。

【0039】なお、上面電極層として銅電極を用いる場合には、焼成温度が600~1000°Cの範囲であれば、抵抗値や抵抗温度係数について再現性が良好であり、銀電極を用いる場合には、焼成温度が600~850°Cの範囲であれば、抵抗値や抵抗温度係数について再

現性が良好である。しかし、銀電極を用いるときに銀と抵抗層の銅との合金化が低温で起こるためにあまり高温には上げられない。また、焼成雰囲気として窒素雰囲気中より還元雰囲気中にて焼成する事によってさらに低抵抗を実現できる。

【0040】(実施の形態3) 図3は本発明の第3の実施の形態のチップ抵抗器の断面模式図を示す。このチップ抵抗器においては、方形の基板1の片面に基板に対向する一対の両端部に下面電極層8をスクリーン印刷などの厚膜技術により印刷焼成して形成する。下面電極層8には金属粉として銅あるいは銀粉を用い、ガラスフリットとして硼珪酸鉛ガラスを金属粉に対して3wt%添加した電極ペーストを用いた。次に、(表3)に示す合金組成になる抵抗体ペーストを用いてスクリーン印刷など\*

\*の厚膜技術により抵抗層3を図3に示すように下面電極層8の上に印刷形成する。次に基板1に対向する一対の両端部に抵抗層3と面接触するように上面電極層2を抵抗層3と同じ方法にて印刷形成する。そしてこの抵抗層3と上面電極層2とを中性雰囲気、もしくは還元雰囲気中にて同時焼成することによって形成する。その後、保護膜および端面電極の形成は実施の形態1と同様な方法にて形成する。

【0041】できたチップ抵抗器の抵抗値、抵抗値の温度係数(TCR)、信頼性(高温放置試験、熱衝撃試験)についても実施の形態1と同様な評価をした。

【0042】

【表3】

合金組成 Cu/Ni (重量比)	比較例 70/30 +ガラスフリット5wt%		70/30 +ガラスフリット5wt%					
	銅粉+ ガラスフリット 5wt%	銀粉+ ガラスフリット 5wt%						
上部電極								
上面電極			銅電極					
下面電極			銅粉+ガラスフリット4%					
焼成温度 (℃)	900	850	600	900	1000	600	900	1000
焼成時間 (時間)	10	10	30	10	10	10	10	10
焼成雰囲気	窒素雰囲気		窒素雰囲気			水素3%-窒素雰囲気		
抵抗値 (mΩ)	60	80	70	30	10	60	20	10
TCR (ppm/℃)	15	40	-20	30	40	-30	20	50
熱衝撃試験 -40℃~ +85℃ 500サイクル	±4%	±5%	±0.4%	±0.2%	±0.1%	±0.4%	±0.2%	±0.1%
高温放置 (150℃- 1000時間)	±5%	±6%	±0.7%	±0.3%	±0.2%	±0.6%	±0.3%	±0.2%

【0043】(表3)から明らかなように、第3の実施の形態によれば、非常に低い抵抗値を有し、熱衝撃特性、耐熱の長期信頼性試験においても非常に優れた抵抗体が得られ、各種電気特性の信頼性も優れている。

【0044】比較例として従来法にて作製された抵抗体は、耐熱性の長期信頼性という観点からは不十分な性能を示した。

【0045】以上のように実施の形態1~3によれば、上面電極層と抵抗層とが合金化された界面を有しているために耐熱特性的に安定な電極構造が得られる低抵抗値、低TCR特性を有し、かつ耐熱性の長期信頼性において抵抗値変化の極めて少ない高精度のチップ抵抗器を実現するとともに、抵抗器を安価に製造できるという有利な効果が得られる。

【0046】なお、実施の形態1~3の厚膜抵抗体組成物は、抵抗値を下げる意味から高温(600~1000℃)での焼成であり、ガラスフリットはガラス転移点が450~800℃の高融点ガラスフリット、特に硼珪酸

鉛ガラス系、硼珪酸亜鉛ガラス系の1種または2種以上が好適である。抵抗温度係数は一般にはゼロに近い方が好ましいため、±400ppm/℃の値が性能、価格などの観点から選択されていたが、本実施の形態により価格・性能比で10倍に近いものが得られた。

【0047】また、基板の材料としては600~1000℃の焼成温度に耐えられるものであればよく、たとえばアルミナ、フォスフェライト、ムライト、窒化アルミニウムのほか、ガラスセラミック系の基板が広く使用できる。

【0048】(実施の形態4) 図4は本発明の第4の実施の形態におけるチップ抵抗器の断面模式図である。図において、3は抵抗層であり、方形のセラミック基板(以下、単に基板と呼ぶ)1の両面に(表4)に示すような合金組成よりなる抵抗体ペーストを用いてスクリーン印刷などの厚膜形成技術により印刷形成している。次にこの抵抗層3の両端部に抵抗層3と面接触するように上面電極層2を抵抗層3と同じ方法で印刷形成し、さら



に基板1の両側面に少なくとも上面電極層2の一部を覆うように一対のコ字状の端面電極層5を形成して、これらを中性雰囲気もしくは還元雰囲気中にて同時焼成している。

【0049】以下に、抵抗体ペーストの作製方法について示す。銅-ニッケル系合金粉は平均粒子径 $2\mu\text{m}$ のアトマイズ粉を用い、これにガラスを添加した混合粉体を無機組成物とした。また、ビヒクルには有機バインダであるエチルセルロースをタービネオールで溶かしたものを、これを有機組成物とした。これらの無機組成物と有機組成物を三本ロールにて混練し、抵抗層3を形成する抵抗体ペーストとした。

【0050】次に、上面電極層2を形成する電極ペーストの作製方法を示す。銅粉は平均粒子径 $2\mu\text{m}$ の粉を用い、これを無機組成物とした。また、ビヒクルには有機バインダであるエチルセルロースをタービネオールで溶かしたものを、これを有機組成物とした。これらの無機組成物と有機組成物を三本ロールにて混練し、上面電極層2用の電極ペーストとした。

【0051】以下に、チップ抵抗器の作製方法について示す。まず抵抗層3用の抵抗体ペーストを基板1(96%アルミナ基板 $6.4\times 3.2\text{mm}$ )の両面に印刷し、 $100^\circ\text{C}$ の温度で10分間乾燥させた。次に、上面電極層\*

\* 2用の電極ペーストを抵抗層3の上面に面接触する構造になるようにスクリーン印刷し乾燥させた。ついで端面電極層5として市販の銅電極ペーストを用いて端面に膜厚約 $50\sim 100\mu\text{m}$ になるように塗布し、その後これらを窒素雰囲気にて $900^\circ\text{C}-10$ 分間焼成して図4のようなチップ抵抗器を作製した。

【0052】以下に、チップ抵抗器の評価方法について示す。チップ抵抗器の上面電極層2間の電極距離を $4.0\text{mm}$ とし、焼成抵抗体の膜幅を $2.5\text{mm}$ で形成し、上面電極層2にプローブを固定して4端子法で端子間抵抗値を求めた。また、TCR特性は、チップ抵抗器を恒温槽に入れて $25^\circ\text{C}$ と $125^\circ\text{C}$ の抵抗値を測定し、その変化率を求めた。高温放置における抵抗値変化は、焼成抵抗体に図10、11に示すような保護層11として樹脂をコート(層厚約 $50\mu\text{m}$ )、 $160^\circ\text{C}$ で1000時間放置したときの抵抗値変化率を求めた。

【0053】作製したチップ抵抗器の断面部を走査電子顕微鏡、電子線マイクロアナライザ、X線微小回折計を用いて構造を明らかにした。

【0054】結果を(表4)に示す。

【0055】

【表4】

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	上面抵抗体膜厚 ( $\mu\text{m}$ )	表面抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR (ppm/ $^\circ\text{C}$ )	高温放置 変化率 (%)
1	70:30:0:0:0	30	100	5.0	80	2.0
2	70:29:1:0:0	30	100	5.2	85	2.0
3	70:29:0:1:0	30	100	5.1	70	2.5
4	70:29:0:0:1	30	100	5.5	60	3.0

【 $900^\circ\text{C}-10\text{min}$ 焼成】

【0056】(表4)より明らかなように本実施の形態のチップ抵抗器によれば、抵抗層を両面に形成することによって低抵抗値、低TCR、高信頼性のチップ抵抗器が得られ、しかも抵抗体層の焼成粒子径が $40\mu\text{m}$ 以下、層厚が $30\mu\text{m}$ 以下のため、YAGレーザーによるトリミングを行うことができる。一般に金属箔や金属線であればレーザーのエネルギーを反射するためレーザートリミングを行うことができず、また、サンドブラスト等のトリミングでは、簡単にしかも高精度のトリミングを行うことができず、本実施の形態のチップ抵抗器は非常に有効的なものである。

【0057】(実施の形態5)図5は本発明の第5の実施の形態におけるチップ抵抗器の断面模式図である。図において、3は抵抗層であり、8は(表5)に示すよう

な合金組成よりなる金属箔8( $6.4\times 3.2\text{mm}$ 、厚さ $=0.04\text{mm}$ )である。

【0058】なお、抵抗層3用の抵抗体ペーストの作製は、実施の形態4と同様の方法で行なった。

【0059】以下に、チップ抵抗器の作製方法について示す。まず抵抗層3を形成する抵抗体ペーストを金属箔8上に印刷し、 $100^\circ\text{C}$ の温度で10分間乾燥させた後、窒素雰囲気にて $900^\circ\text{C}-10$ 分間焼成し、図5のようなチップ抵抗器を作製した。

【0060】チップ抵抗器の評価方法については、実施の形態4と同様の方法で行ない、その結果を(表5)に示す。

【0061】

【表5】

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属箔組成表 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
5	70:30: 0: 0: 0	70:30: 0: 0	30	3.0	80	2.0
6	70:30: 0: 0: 0	70:29: 1: 0	30	4.0	85	2.0
7	70:30: 0: 0: 0	0:95: 5: 0	30	3.4	70	2.6
8	70:30: 0: 0: 1	0:95: 4: 1	30	3.5	60	3.0

[900℃-10min焼成]

【0062】(実施の形態6) 図6は本発明の第6の実施の形態におけるチップ抵抗器の断面模式図である。図において3は抵抗層で、8は(表6)に示すような金属箔であり、方形の基板1の両面に(表6)に示すような合金組成よりなる抵抗体ペーストを用いてスクリーン印刷などの厚膜形成技術により印刷形成している。次に、この抵抗層3の両端部に抵抗層3と面接触するように上面電極層2を抵抗層3と同じ方法で印刷形成し、さらに基板1の両側面に少なくとも上面電極層2の一部を覆うように一對のコ字状の端面電極層5を形成してこれらを中性雰囲気もしくは還元雰囲気中にて同時焼成している。

【0063】なお、抵抗層3用の抵抗体ペーストの作製および上面電極層2用の電極ペーストの作製については、実施の形態4と同様の方法で行なった。

【0064】以下に、チップ抵抗器の作製方法について\*

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属箔組成表 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
9	70:30: 0: 0: 0	70:30: 0: 0	30	4.0	80	2.0
10	70:30: 0: 0: 0	70:29: 1: 0	30	5.0	85	2.0
11	70:30: 0: 0: 0	0:95: 5: 0	30	4.4	70	2.6
12	70:30: 0: 0: 1	0:95: 4: 1	30	4.5	60	3.0

[900℃-10min焼成]

【0067】(実施の形態7) 図7は本発明の第7の実施の形態におけるチップ抵抗器の断面模式図である。

【0068】なお、本実施の形態は、第6の実施の形態の金属箔8に代え、(表7)に示されるような金属線9を用いた例を示しており、金属線9として直径=0.6mm、長さ=3.8mmのものを、基板1上に設けられたスリット(図示せず)にはまり込めるように構成され\*

示す。まず基板1(96%アルミナ基板6.4×3.2mm)上に金属箔8(3.8×2.3mm、厚さ=0.02mm)を接着等で固定させ、その上に抵抗層3を形成する抵抗体ペーストを印刷し、100℃の温度で10分間乾燥させた。次に、上面電極層2を形成する電極ペーストを抵抗層3の上面に面接触する構造になるようにスクリーン印刷し乾燥させた。次に端面電極層5として市販の銅電極ペーストを用いて端面に膜厚約50~100 $\mu\text{m}$ になるように塗布し、その後これらを窒素雰囲気にて900℃-10分間焼成して図6のようなチップ抵抗器を作製した。

【0065】チップ抵抗器の評価方法については、実施の形態4と同様の方法で行ない、その結果を(表6)に示す。

【0066】

【表6】

30※している。

【0069】チップ抵抗器の評価方法については、実施の形態4と同様の方法で行ない、その結果を(表7)に示す。

【0070】

【表7】

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属線組成表 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 ( $\mu\text{m}$ )	端子間抵抗値 ( $\text{m}\Omega$ )	TCR ( $\text{ppm}/^\circ\text{C}$ )	高温放置 変化率 (%)
13	70:30: 0: 0: 0	70:30: 0: 0	30	2.0	80	2.0
14	70:30: 0: 0: 0	70:29: 1: 0	30	2.5	85	2.0
15	70:30: 0: 0: 0	0:95: 5: 0	30	2.2	70	2.6
16	70:30: 0: 0: 1	0:95: 4: 1	30	2.8	60	3.0

[900℃-10min焼成]

【0071】(実施の形態8) 図8は本発明の第8の実施の形態におけるチップ抵抗器の断面模式図である。図において3は抵抗層で、8は(表8)に示すような金属箔であり、方形の基板1のもう一方の片面には(表8)に示すような合金組成よりなる抵抗体ペーストを用いてスクリーン印刷などの厚膜形成技術により印刷形成して

いる。次に、この抵抗層3の両端部に抵抗層3と面接触するように上面電極層2を抵抗層3と同じ方法で印刷形成し、さらに基板1の両側面に少なくとも上面電極層2の一部を覆うように一對のコ字状の端面電極層5を形成して、これらを中性雰囲気もしくは還元雰囲気中にて同時焼成している。

【0072】なお、抵抗層3用の抵抗体ペーストの作製および上面電極層2用の電極ペーストの作製については、実施の形態4と同様の方法で行なった。

【0073】以下にチップ抵抗器の作製方法について示す。まず基板1（96%アルミナ基板6.4×3.2mm）の片面に金属箔8（6.4×2.5mm、厚さ=0.1mm）を接着等で固定し、抵抗層3を形成する抵抗体ペーストを金属箔8とは反対の面に印刷し、100℃の温度で10分間乾燥させた。次に上面電極層2を形成する電極ペーストを抵抗層3の上面に面接触する構造になる\*10

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属箔組成 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 (μm)	端子間抵抗値 (mΩ)	TCR (ppm/℃)	高温放置 変化率 (%)
17	70:30:0:0:0	70:30:0:0:0	30	1.0	100	2.0
18	70:30:0:0:0	70:29:1:0:0	30	1.2	85	2.0
19	70:30:0:0:0	0:95:5:0:0	30	1.1	90	2.8
20	70:30:0:0:0	0:95:4:1:0	30	1.0	80	3.0

【900℃-10min焼成】

【0076】（実施の形態9）図9は本発明の第9の実施の形態におけるチップ抵抗器の断面模式図である。図において3は抵抗層で、9は（表9）に示すような金属線であり、方形の基板1の両面に（表8）に示すような合金組成よりなる抵抗体ペーストを用いてスクリーン印刷などの厚膜形成技術により印刷形成している。次に、この抵抗層3の両端部に抵抗層3と面接触するように上面電極層2を抵抗層3と同じ方法で印刷形成し、さらに基板1の両側面に少なくとも両面に設けられた上面電極層2の一部を覆うように一対のコ字状の端面電極層5を形成して、これらを中性雰囲気もしくは還元雰囲気中に同時焼成している。

【0077】なお、抵抗層3用の抵抗体ペーストの作製および上面電極層2用の電極ペーストの作製については実施の形態4と同様の方法で行なった。

【0078】以下に、チップ抵抗器の作製方法について示す。まず基板1（96%アルミナ基板6.4×3.2×

\*ようにスクリーン印刷形成し乾燥させた。ついで端面電極層5として市販の銅電極ペーストを用いて端面に膜厚約50～100μmになるように塗布し、その後、これらを窒素雰囲気にて900℃-10分間焼成して図8のようなチップ抵抗器を作製した。

【0074】チップ抵抗器の評価方法については、実施の形態4と同様の方法で行ない、その結果を（表8）に示す。

【0075】

【表8】

※mm）の片面に設けられたスリット（図示せず）に金属線9（直径=0.6mm、長さ=3.8mm）を挿入固定する。次に、抵抗層3を形成する抵抗体ペーストをその両面に印刷し、100℃の温度で10分間乾燥させた。次に、上面電極層2を形成する電極ペーストを両抵抗層3の上面に面接触する構造になるようにスクリーン印刷形成し乾燥させた。ついで端面電極層5として市販の銅電極ペーストを用いて端面に膜厚約50～100μmになるように塗布し、その後、これらを窒素雰囲気にて900℃-10分間焼成して図9のようなチップ抵抗器を作製した。

【0079】チップ抵抗器の評価方法については、実施の形態4と同様の方法で行ない、その結果を（表9）に示す。

【0080】

【表9】

No.	抵抗体組成 (wt%) Cu: Ni: Mn: Cr: Fe	金属線組成 (wt%) Cu: Ni: Mn: Cr: Al	焼結抵抗体膜厚 (μm)	端子間抵抗値 (mΩ)	TCR (ppm/℃)	高温放置 変化率 (%)
21	70:30:0:0:0	70:30:0:0:0	30	1.5	80	2.0
22	70:30:0:0:0	70:29:1:0:0	30	1.7	65	2.0
23	70:30:0:0:0	0:95:5:0:0	30	1.6	70	2.8
24	70:30:0:0:0	0:95:4:1:0	30	1.5	60	3.0

【900℃-10min焼成】

【0081】なお、実施の形態4～9では端面電極層5として上表面抵抗体の導通をとる例について示したが、基板1にスルーホール等を形成し金属ペーストや金属を埋めて導通させて低抵抗チップ抵抗器を形成することも可能である。また、金属箔あるいは金属線を用いる場合、基板1に凹凸（スリット）をつけて凹部に金属箔、金属線を固定して抵抗器を形成すると接着等の手間が省けるとともに、接着剤に含まれる特性に影響を与えるような物質を用いずにそれらを確実に固定することがで

き、非常に有効である。

【0082】また、本実施の形態では、YAGレーザーによるトリミングの例を説明したが、その他のレーザーによるトリミングを行なっても同様の効果が得られることは言ういうまでもなく、抵抗体層の膜厚をそのレーザーによるトリミングが可能な範囲に形成すればよく、特に焼成粒子径が40μm以下、層厚が30μm以下の場合が好ましいことが実験的に見い出されている。

【0083】

【発明の効果】以上のように、本発明によれば、抵抗層と上面電極層の接合が金属接合で行なわれるため、その界面には特性に影響を与えるような不純物が介在せず、銅／ニッケル合金の材料特性を十分に生かした低抵抗、低TCR特性を有し、かつ耐熱特性に優れた高信頼性の優れたチップ抵抗器が実現できる。

【0084】また、焼成抵抗体層の焼結粒子径を30 $\mu$ m以下で、かつその膜厚が40 $\mu$ m以下になるように構成されているため、レーザーによるトリミングが可能となり、サンドブラスト等による研磨に比べ非常に簡単にしかも精度良くトリミングを行なうことが可能となり、非常に安価でかつ高精度のチップ抵抗器が実現できる。

【図面の簡単な説明】

【図1】本発明の第1の実施の形態におけるチップ抵抗器の模式断面図

【図2】同実施の形態の製造工程図

【図3】本発明の第3の実施の形態におけるチップ抵抗器の模式断面図

【図4】本発明の第4の実施の形態におけるチップ抵抗器の模式断面図

【図5】本発明の第5の実施の形態におけるチップ抵抗器の模式断面図

【図6】本発明の第6の実施の形態におけるチップ抵抗器\*

\* 器の模式断面図

【図7】本発明の第7の実施の形態におけるチップ抵抗器の模式断面図

【図8】本発明の第8の実施の形態におけるチップ抵抗器の模式断面図

【図9】本発明の第9の実施の形態におけるチップ抵抗器の模式断面図

【図10】本発明の第4の実施の形態におけるチップ抵抗器に保護層として樹脂コーティングが施された様子を示す斜視図

【図11】同一部切欠断面図

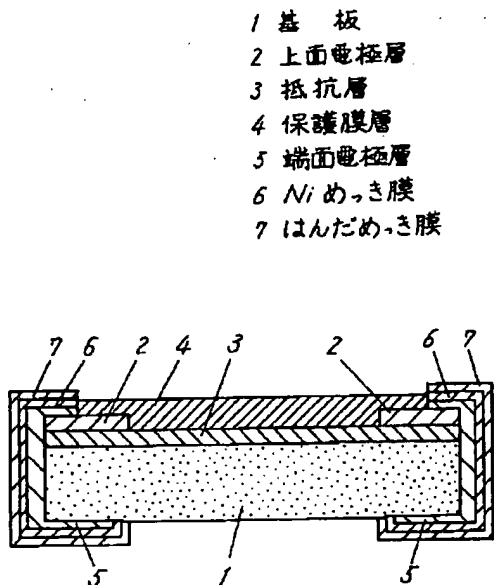
【図12】従来のチップ抵抗器の構成を示す斜視図

【図13】同A-A'断面図

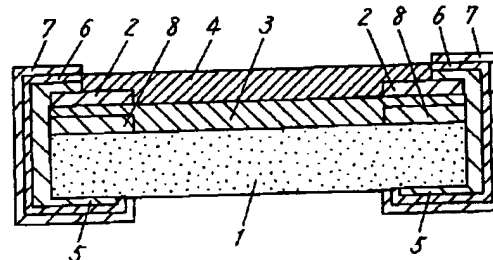
【符号の説明】

- 1 基板
- 2 上面電極層
- 3 抵抗層
- 4 保護膜層
- 5 端面電極層
- 6 Niめっき膜
- 7 はんだめっき膜
- 8
- 20

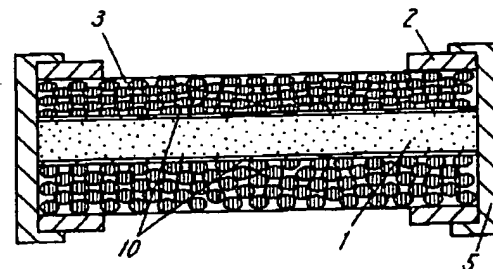
【図1】



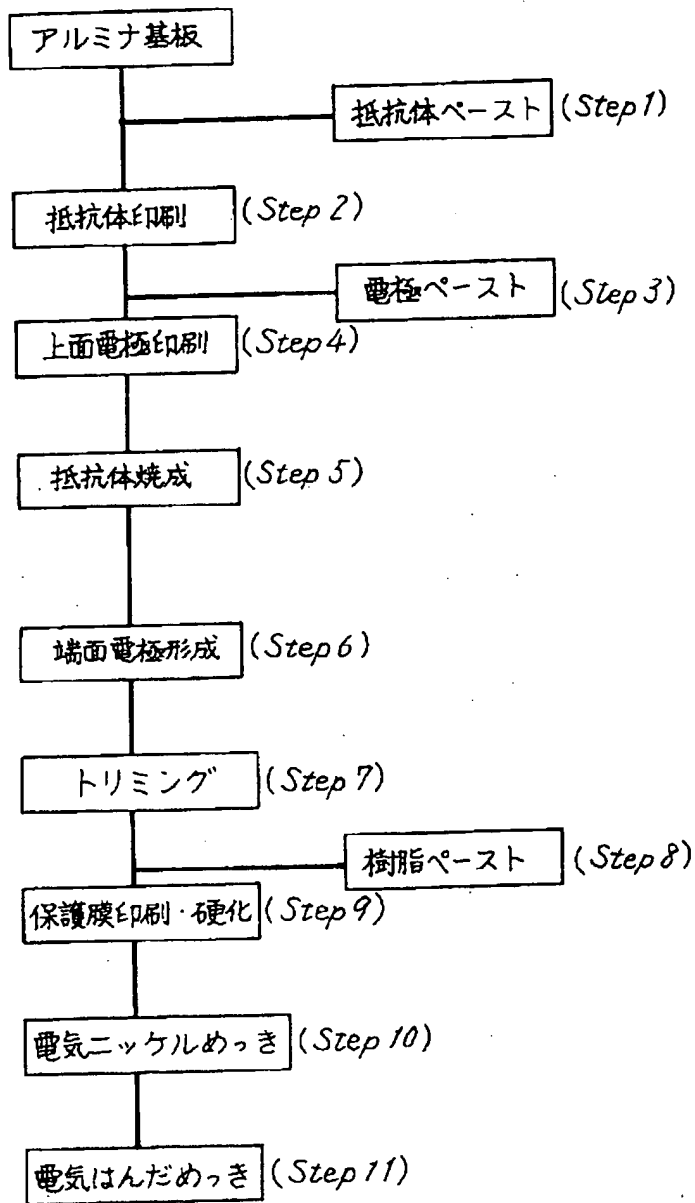
【図3】



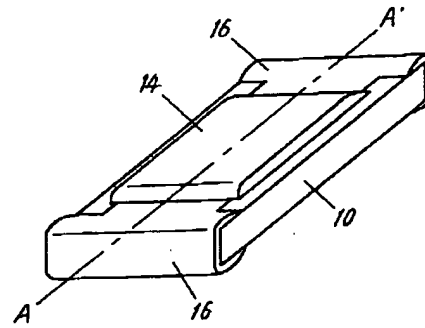
【図4】



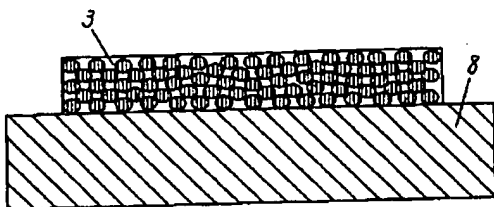
【図2】



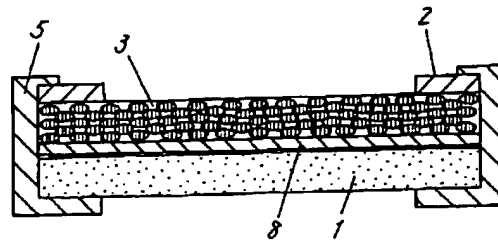
【図12】



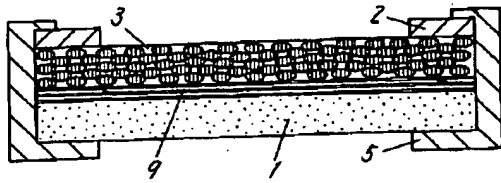
【図5】



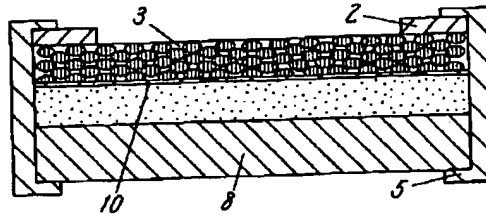
【図6】



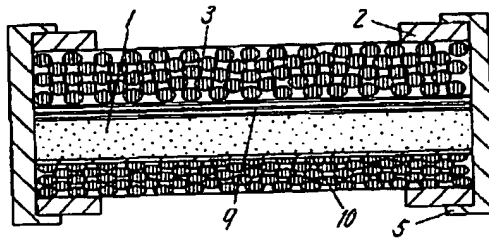
【図7】



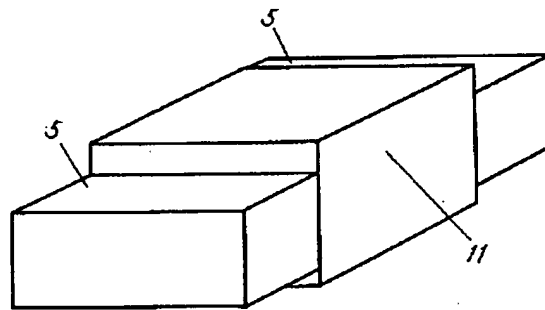
【図8】



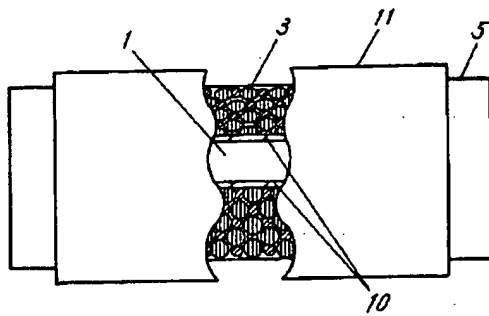
【図9】



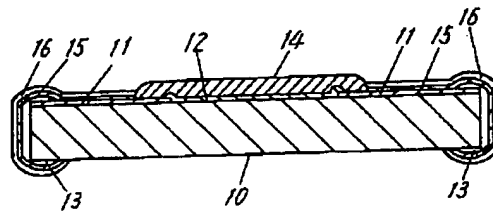
【図10】



【図11】



【図13】



フロントページの続き

(72)発明者 米田 尚継  
大阪府門真市大字門真1006番地 松下電器  
産業株式会社内

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